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CCD Modelling and Verification for ESA's Euclid CCD Architecture

Thesis submitted for the degree of

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by

Andrew Clarke BEng (Hons).

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Discipline of Planetary and Space Science

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Abstract

This thesis discusses semiconductor modelling carried out to investigate the charge packets which are present in Charge Coupled Devices (CCDs). The details of charge distribution are of interest for scientific CCDs, in particular those which may become damaged due to the effects of harsh radiation environments such as those experienced in space. Therefore this thesis focuses on the CCDs used in the main focal plane instrument (VIS, a visible imager) on the European Space Agency's Euclid space telescope due for launch in 2018.

The thesis is split into two parts, with the early chapters concentrating on the development of device models and the interpretation of modelling results. The modelling work is verified in latter chapters to ensure that the model predictions concur with lab based measurements on test devices.

Model verification makes up a large part of this thesis, ensuring the accuracy of the models. In some cases initial modelling work was shown to predict parameters different to those measured in test devices, however, investigations are made which show manufacturing errors are partly to blame. During this work images were taken using a Focussed Ion Beam Scanning Electron Microscope (FIBSEM), which allows cross-sectional images of the device to be taken, these showed deviations from the designed poly silicon electrode geometry, resulting in some undersized and some oversized gates, these reduced the accuracy of some models, which were later modified. Through this investigation a method for predicting gate geometry was developed based on the Silvaco device models.

Further testing was carried out to verify the charge packet relationship with CTE in test devices. CTE is measured using the Extended Pixel Edge Response (EPER) technique, which allows CTE to be measured over a range of signal sizes. The CTE data can be used to calculate the charge loss per pixel as an average across the device column and these values can be compared against the charge packet volume simulations.

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Thanks to David Burt for imparting fractions of his vast knowledge and experiences on me.

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Thanks to the current and former members of the CEI, Ben Dryer, Anthony Evagora, Richard Harriss, Phillipa Smith, Mathew Soman, James Tutt, Edgar Allanwood, Jason Gow, Ross Burgon, Calum MacCromick and Tom Grieg who provided friendship, entertainment and insight over my time with the group.

Declaration

I hereby declare that no part of this thesis has been previously submitted to this or any other university as part of the requirement for a higher degree. The work described herein was conducted solely by the undersigned except for those colleagues and other workers acknowledged in the text.

Andrew Clarke

List of Publications

A. S. Clarke; D. J. Hall; A. Holland and D. Burt; (2012). Modelling charge storage in Euclid CCD structures. *Journal of Instrumentation*, Vol. 7. C01058 doi:10.1088/1748-0221/7/01/C01058

A. Clarke; D. Hall; N. Murray; A. Holland; D. Burt; (2012). Device modelling and model verification for the Euclid CCD273 detector. Proc. SPIE 8453, *High Energy, Optical, and Infrared Detectors for Astronomy V*, 84531I; doi:10.1117/12.925887.

A. Clarke; D. Hall; N. Murray; J. Gow; A. Holland; D. Burt; (2014). Pixel-level modelling and verification for the EUCLID VIS CCD. Proc. SPIE 8860, *UV/Optical/IR Space Telescopes and Instruments: Innovative Technologies and Concepts VI*, 88600V; doi:10.1117/12.2024045.

Tutt, James H; Holland, Andrew D; Murray, Neil J; Hall, David J; Harriss, Richard D; **Clarke, Andrew** and Evagora, Anthony M (2012). The noise performance of electron-multiplying charge-coupled devices at soft X-ray energy values. *IEEE Transactions on Electron Devices*, 59(8) pp. 2192–2198.

Gow, J. P. D.; Murray, N. J.; Hall, D. J.; **Clarke, A. S.**; Burt, D.; Endicott, J. and Holland, A. D. (2012). Assessment of proton radiation-induced charge transfer inefficiency in the CCD273 detector for the Euclid Dark Energy Mission. *High Energy, Optical, and Infrared Detectors for Astronomy V*, 1-6 July 2012, Amsterdam.

Hall, David J.; Holland, Andrew; Murray, Neil; Gow, Jason and **Clarke, Andrew** (2012). Modelling charge transfer in a radiation damaged charge coupled device for Euclid. In: *High Energy, Optical, and Infrared Detectors for Astronomy V*, 01-06 July 2012, Amsterdam.

Greig, T., Stefanov, K., Holland, **A., Clarke**, A., Burt, D., & Gow, J. (2013). "Total ionizing dose effects on IV and noise characteristics of MOS transistors in a 0.18 μm CMOS Image Sensor process." *Radiation and Its Effects on Components and Systems (RADECS), 2013 14th European Conference on*. IEEE, 2013.

Hall, David J.; Murray, Neil J.; Holland, Andrew D.; Gow, Jason; **Clarke, Andrew** and Burt, David (2014). Determination of in situ trap properties in CCDs using a "single-trap pumping" technique. *IEEE Transactions on Nuclear Science*, 61(4) pp. 1826–1833.

Technical Notes

A. Clarke, 2012. Euclid Pixel Modelling, The Supplementary Buried Channel. *Technical Note, Open_Euclid_TN_25*.

A. Clarke, 2011. Euclid CCD273 Device, 3D Modelling of Charge Storage in the CCD273 and the previous CCD204. *Technical Note, Open_Euclid_TN_21*.

Acronyms

ADC	Analogue-to-Digital Converter
ADU	Analogue to Digital Units
AF	Astronometric Field
APS	Active Pixel Sensor
BBD	Bucket Brigade Device
CAD	Computer Aided Design
CCD	Charge Coupled Device
CDM	Charge Distortion Model
CMOS	Complementary Metal Oxide Semiconductor
CTE	Charge Transfer Efficiency
CTI	Charge Transfer Inefficiency
DN	Digital Number
EPER	Extended Pixel Edge Response
ESA	European Space Agency
FIBSEM	Focussed Ion Beam Scanning Electron Microscope
FPA	Focal Plane Array
FPN	Fixed Pattern Noise
FWC	Full Well Capacity
HST	Hubble Space Telescope
IC	Integrated Circuit
L2	Lagrange Point 2
LED	Light Emitting Diode
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NASA	National Aeronautics and Space Administration
NIR	Near Infra-Red
NISP	Near Infra-Red Spectrometer and Photometer

PSF	Point Spread Function
PTC	Photon Transfer Curve
RMS	Root Mean Squared
ROI	Region of Interest
RVS	Radial Velocity Sensor
SBC	Supplementary Buried Channel
SM	Sky Mapper
SRH	Shockley -Read-Hall
STFC	Science and Technology Facilities Council
TCAD	Technology Computer Aided Design
TDI	Time Delay Integration
TV	Television
WL	Weak Lensing

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Chapter 1: Introduction

This thesis is a record of work funded by a Co-operative Award in Science and Engineering (CASE) studentship awarded by the Science and Technology Facilities Council (STFC) and in collaboration with e2v technologies Plc. The work presented here is in support of the Euclid CCD development and characterisation carried out by e2v technologies Plc. and the centre for electronic imaging based at the Open University.

1.1 The Charge Coupled Device

Charged Coupled Devices, CCDs, were first developed in the early 1970s by Boyle and Smith of Bell Labs (Janesick, 2001) using Metal Oxide Semiconductor (MOS) technology. This was early in the history of semiconductors; roughly ten years after the first MOS transistors were developed. Many uses were suggested for the new CCD technology, but it was realised that the CCD would form an efficient photo-sensitive substrate, which could be used in a digital camera system. By the end of the decade the first TV resolution CCDs were produced, and by the early 1980s the first CCDs were being developed for use in astronomy and spectroscopy with designs which enhanced the image intensities. NASAs 1989 Galileo mission to Jupiter pioneered the use of CCD technology in space (Baerg, 2010). However, it wasn't until the 1990s, with the development of the Hubble Space Telescope (HST) (Hille, 2013), that large area arrays for astronomical applications developed a reputation for highly reliable, low power space based imaging.

An alternative technology known as the CMOS Active Pixel Sensor (CMOS-APS) has been developed by the solid state imaging industry in parallel with the CCD. The CMOS-APS has become the dominant detector for most consumer imaging applications, and is used in mobile telephones and digital cameras due to the integration of signal processing circuits on chip and low cost, large scale manufacture. However, the CCD technology is still favoured for scientific imaging due to the high optical quality of specialised CCD manufacturing processes, better noise performance, low cost development for small volumes of detectors relative to CMOS and high technology readiness level (TRL).

1.2 Space Telescopes

Space-based telescopes improve sensor performance over ground based astronomy by removing the distorting effects of a turbulent atmosphere (Cropper, et al., 2012). However the space environment introduces other problems into the detector system, such as the potential for large temperature swings and a severe radiation environment. CCD images can be distorted by the effects of the Charge Transfer Inefficiency (CTI) which is caused by the interaction between the collected signal and trap sites in the silicon lattice. Unfortunately, the space radiation environment increases the number of traps within solid state detectors, gradually degrading the detector's performance over its lifetime.

Charge Transfer Inefficiency (CTI) caused by bulk trapping states may cause distortion to captured images, or a loss of signal, causing degradation in the signal to noise ratio of the detector system. Although there are methods to mitigate the effects of radiation damage, it is not possible to prevent it. There has, however, been some advancement in the understanding of these effects which have allowed the post-processing of images to remove the effects of CTI (Massey, 2010) (Short, et al., 2012). The work in this thesis forms a method for modelling devices and hence predicting the radiation performance of the detectors through the distribution of charge packets, with an aim to improve the understanding of charge trapping and the causes of CTI.

1.3 Research Goals

This thesis was developed during the development and characterisation stages for the detector used in the Euclid visible (VIS) focal plane, namely the e2v CCD273. The work contained in this thesis was undertaken with the aim of developing the understanding of charge storage mechanisms within the detectors that might affect device performance, or the reconstruction of galaxy shapes. This work addresses the questions that were left unanswered from modelling and characterisation which was performed for the Gaia detectors and the development of the Charge Distortion Model, CDM (Short, et al., 2012). The main aims of this thesis are to develop device models which give insight into the characteristic "charge cloud" and how device parameters, and

radiation damage, may affect its distribution and the way charge interacts within the device structure.

Without methods for CTI correction it would not be possible to produce accurate astronomical data from space based telescopes. The weak lensing survey (Amendola, et al., 2012) which will be performed by the Euclid mission, requires particularly accurate measurements of the shapes of galaxies. Previous work in the area of CTI correction has focussed on analysing data from detectors in an effort to remove charge tails and restore images. Little work has been done to investigate the charge distribution in CCDs from a CTI perspective, which this thesis addresses.

A number of studies were carried out to verify the device model parameters. As the models were primarily investigating the evolution of the charge packet, the parameters used to verify the models are directly related to the charge packet, including an in-depth study of the Full Well Capacity (FWC) parameter extracted from the photon transfer measurements. These studies, along with images of the gate structure of the CCD273, obtained through Focussed Ion Beam Scanning Electron Microscope (FIBSEM) analysis yielded some interesting information about the manufacture of the CCDs, and highlighted some problems concerning the electrode deposition and possibly device operation.

1.4 Thesis Organisation

The thesis is organised into 8 Chapters including this introductory chapter. After the background and theory chapters, the work completed for presentation in this thesis is described. Each chapter describes a separate study which is focussed on modelling CCDs for the Euclid space mission or testing devices to confirm the model findings.

Chapter 2 gives background information about CCDs used in space based astronomical telescopes, with particular attention on recent and future European Space Agency (ESA) missions, Gaia and Euclid, along with a brief overview of the instruments and the detectors used. Chapter 2 discusses the science goals of Euclid and Gaia and how they may be affected by radiation damage in the space environment. Common silicon trap species are described with reference to Shockley-Read-

Hall trapping theory. Methods to mitigate and correct for radiation damage effects are described with examples from the Hubble Space Telescope (HST) and a description of the methods which will be used as part of the Gaia data processing.

Chapter 3 gives an introduction to solid state imaging through the use of the CCD. The chapter gives an overview of CCD architecture and operation. A basic knowledge of semiconductors is assumed, so the basic operational theory of the CCD is described through a description of its constituent parts, the MOS capacitor and the buried pn-junction. The pixel architecture is described, showing the channel isolation and gate layout. An overview of the whole detector is presented, showing the relative positions of the parallel and serial registers. The potential well model is introduced so that charge transfer through manipulation of the gate biases can be described. Examples are used to describe a simple, single stage output amplifier, and the more complex two stage amplifier which is used in the Euclid detectors. Chapter 3 goes on to describe some of the common noise sources in the CCD, which are important in the understanding the measurements made in later chapters. The chapter ends with some technical information about the two detectors used and modelled in this study, the CCD204 and the CCD273.

Chapter 4 is the first chapter to introduce the modelling techniques used throughout this thesis. It describes the initial production of the models from CAD drawings, and how the model may be set up for greater accuracy or speed, giving examples. The chapter goes on to describe how model results should be interpreted by the user and how some of the parameters, which are used to verify the models in later chapters, are defined.

Chapter 5 describes the Silvaco device models developed for this study and shows how the charge packet information might be extracted from device models. Examples are given for the charge packet evolution over the entire signal range as extracted from the Silvaco models. How this information might be integrated into charge transfer models is then discussed through the use of Shockley-Read-Hall Theory (Shockley & Read , 1952). Descriptions of how the charge packet is stored in a range of structures are made, showing larger, more diffuse charge packets in larger

devices for a given signal size. The chapter ends with a section showing the possible effects of a Supplementary Buried Channel (SBC) on the charge packet of the Euclid pixel, drawing parallels with the Gaia device.

Chapter 6 covers measurements of FWC made using an e2v CCD204 test device. The CCD204 shares the same pixel design as the CCD273 used in Euclid, so should offer comparable results in FWC measurements. The chapter includes an in-depth description of the FWC measurement using a Photon Transfer Curve (PTC) and the noise sources present in the detector that governs the measurement. FWC was chosen as a primary parameter to verify the device models because it is directly related to the charge storage characteristics, which are the ultimate aim of this study. The FWC extracted from the models is initially much larger than the values modelled, but after taking account of the deviation in gate geometry from the expected measurements, as seen in the FIBSEM measurements the values form much closer agreement. The test device and the device images in the FIBSEM study come from different devices which were manufactured in different batches several years apart, so the gate dimensions may not be common across the two. A definitive confirmation of the gate dimensions in the test device cannot be made, but gate dimensions may be estimated when comparing model FWC values to those measured in a test device. This gives a method for estimating gate dimensions without the use of destructive testing, such as a FIBSEM analysis.

Chapter 7 presents measurements made using the Extended Pixel Edge Response (EPER) technique, to estimate the CTE on a CCD273 test device. The EPER technique provides a method for calculating a relative value for CTE over a large signal range by analysing the amount of deferred charge in the overscan regions of a flat field image. Obtaining values for CTE over a range of signal sizes enables charge loss to be calculated and compared against the trends observed for the charge packet models in Chapter 5, to confirm the links between charge loss and charge packet distribution.

Chapter 8 provides the final conclusions of the thesis, summarising the findings from each chapter and briefly outlining the impact these results might have on the Euclid mission and its science objectives and suggesting possible directions for future work.

Chapter 2: Precision Astronomy using CCDs.

This chapter reviews two current European Space Agency (ESA) missions which include CCD focal plane arrays as part of the main instruments. The older Hubble space telescope is also introduced, because many of the radiation damage effects and correction techniques described in this thesis were first developed for the Hubble Space Telescope. Brief descriptions of the European mission aims are given before a description of the detector layout and operational parameters governing the achievement of the mission goals. Finally the space radiation environment is discussed and its effects on the detector operation along with its impact on the missions' science goals.

2.1 The Hubble Space Telescope

The Hubble Space Telescope (HST) was developed and is operated by National Aeronautics and Space Administration (NASA). Named after the famous astronomer Edwin Hubble, the telescope consists of four instruments which make observations in the near infra-red, near ultra-violet and visible wavelengths (Hille, 2013). The HST was launched in 1990 and is located in a low earth orbit, where the distorting effects of the atmosphere are eliminated enabling more accurate imaging. This location allows the telescope to be serviceable by astronauts who have upgraded the instruments several times over the mission lifetime.

The radiation damage effects experienced by the Hubble CCDs have been studied in detail over the last two decades, but have been partially mitigated by the replacement instruments which have been installed. An example of recent work on Hubble data correction is given in later sections of this chapter (Massey, 2010).

2.2 The Gaia Mission

Gaia is a major cornerstone mission of the European Space Science Program. In its five year operational lifetime, the orbital telescope aims to map accurate values for the three dimensional positions and velocities of stars throughout the Milky Way, including the galactic disk and the bulge at the galactic centre (de Bruijne, et al., 2010). Gaia is a space based telescope, Figure 2.1, orbiting the L2 point of the Sun-Earth/Moon system roughly 1.5 million km from Earth (de Bruijne,

et al., 2010). L2 offers a stable thermal environment, low radiation environment and a high observing efficiency (de Bruijne, et al., 2010). The telescope will consist of a large focal plane mosaic made up of 106 CCDs, with a total area of approximately 0.5 m x 1 m which perform three functions: astrometry, photometry and spectroscopy (de Bruijne, et al., 2010).

Gaia was successfully launched in December 2013 from a European Space Agency launch facility in French Guiana. After several months of calibrations and commissioning the first observations were made in summer 2014.

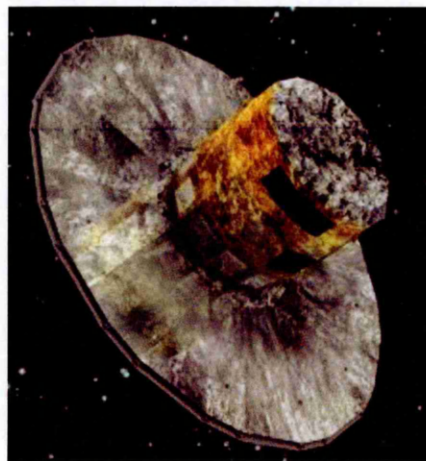


Figure 2.1: Artists impression of the Gaia space telescope. The spacecraft dimensions are approximately 4.6 m x 2.5 m.

The main aims of the Gaia mission are to derive a history of star formation from observed populations and to identify cosmic structures and the dynamics of the galaxy. The measurements are dependent on a repeated systematic all sky observation of star positions, achieved because the CCDs are constantly imaging as the spacecraft slowly rotates about its axis. Coverage of the entire sky is achieved after approximately 3 months. At the end of mission, scientists expect to obtain 70 relative position measurements for each of 1000 million stars, which should give a complete determination of the astrometric parameters, angular position, motion and distance, among other information (de Bruijne, et al., 2010).

The CCDs which make up Gaia's focal plane are large area devices ($\sim 26.5 \text{ cm}^2$), operated in Time Delay Integration (TDI) mode, where the CCD readout period is synchronised with the spacecraft

motion (Short, 2004). A light source of interest moves across the mosaic in the Along Scan (AL) direction indicated in Figure 2.2 (Dell'Oro & Cellino , 2012), in sequence with the CCD charge transfer process, allowing charge to continue to accumulate during readout. Signal sources are windowed as they move across the Astrometric Field (AF) CCDs after they are initially detected by the Sky Mapper (SM) CCDs, Figure 2.2.

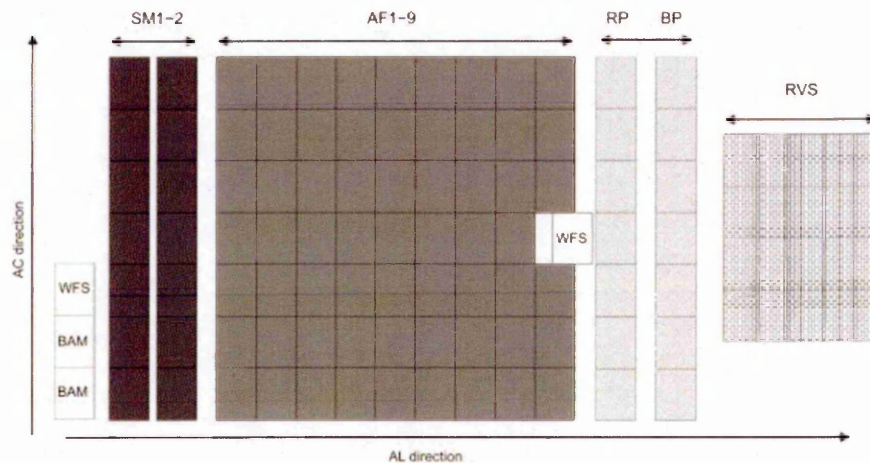


Figure 2.2: The focal plane of the Gaia telescope measuring $\sim 0.5\text{m} \times 1\text{m}$. The charge is readout of these devices in synchronisation with the spacecraft rotation in TDI mode. Objects of interest are initially detected by the Sky Mapper (SM) CCDs, then windowed as they cross the Astronometric Field (AF) CCDs. There is also a Radial Velocity Sensor (RVS), Wave Front Sensor (WFS), Basic Angle Measure (BAM) and Blue and Red Photometers (BP and RP) (Dell'Oro & Cellino , 2012).

As in all space-based CCDs, Gaia's detectors face problems relating to an increase in charge transfer inefficiency caused by the effects of the space radiation environment. In Gaia's case, the effects of CTI will be calibrated out of the images by the on-ground post-processing centred around the Charge Distortion Model (CDM) (Short, et al., 2012), which is based on Shockley-Read-Hall theory (Hardy, et al., 1998) (Shockley & Read , 1952) and is discussed in more detail in later chapters.

The Gaia CCDs also contain technology designed to mitigate the effects of radiation damage on Charge Transfer Efficiency (CTE). One of the mechanisms for reducing CTI is a charge injection

structure, which can be used to move a known amount of charge through the detectors before an image is captured and read out. This will have the effect of filling a large portion of the traps which are present in the detector before an image of interest is captured, preventing the traps from interacting with the charge packets which make up the image and thus improving performance. However this will only eliminate traps which have longer emission times.

The second mechanism is a SBC which exists within the normal buried channel structure of the image area (Seabroke, et al., 2013). This runs the entire length of each of the parallel registers and works to confine charge to a smaller cross-section at small signal levels, where the small cross-section of a charge packet should lead to fewer trap interactions and has been shown to improve CTE (Seabroke, et al., 2013). The SBC is implemented due to the relatively large size of the pixel structure, allowing the SBC to potentially make a substantial difference.

2.3 The Euclid Mission

Euclid is an M-class mission selected for the next phase of ESA's long-term cosmic vision programme (2015-2025) (Laureijs, et al., 2011). The mission will create survey images over approximately one third of the sky using a telescope feeding light to several instruments. It is dedicated to investigating dark energy and dark matter, which will be achieved through two main mission surveys. The two surveys are analysing weak lensing, which focuses on the distortion of a galaxies' visible light, and galaxy clustering, the interaction between galaxies (Laureijs, et al., 2012). With a planned launch in 2020, Euclid has a primary aim to provide insight into the physical cause of the accelerating universe which is theorised to be caused by the influence of dark energy (Cropper, et al., 2012).

The instruments on board Euclid include both a visible 'VIS' detector made up of an array of e2v CCD273s used for the Weak Lensing (WL) survey, and Near Infrared Spectrometer and Photometer (NISP) instruments (Prieto, et al., 2012). During the planned six year lifespan the mission will produce a map of both the light and dark components of the universe in a wide field survey covering one third of the sky (~2 billion galaxies) and a deeper narrow field survey on ~1/1000 of the sky (~100 million galaxies). The narrow field survey will investigate the evolution

of cosmic structure by measuring galaxy clustering using the deep field Near Infra-Red (NIR) imager. NIR will map the 3D position and red shifts of galaxies over a survey area of approximately 100 million galaxies. The unique combination of probes present on the Euclid mission provides a cross-checking capability needed for high precision measurements (Laurejis, et al., 2012).

The weak lensing survey depends on the analysis of the average distortion in millions of galaxy shapes, through this survey scientists hope to extract a 3D map of the energy and mass densities of the Universe. WL should provide 3D maps of the distribution of dark matter and constrain the properties of dark energy for further study. On top of the mission aims, large, highly detailed survey datasets will be formed, which will be available to the wider cosmology and physics communities giving high resolution images, spectra and redshifts of approximately 50 million galaxies (Amendola, et al., 2012).

This thesis focuses on modelling and analysis of the CCD273 used to produce the VIS detector array, with some work also detailing the predecessor to the CCD273, the CCD204. The Point Spread Function (PSF) of the CCD273 is an important parameter for an accurate WL survey, but it is adversely affected by the CTI introduced by radiation damage in the detector. This thesis aims to explore and understand some of the device parameters that may affect the PSF through CTI, and hence the WL survey.

2.3.1 Weak Lensing

Weak lensing, or cosmic shear, is an astronomical effect where the light from distant galaxies is distorted by a large mass that might exist between the light source and the observer. The light becomes distorted due to the effect of the gravity of the intervening mass on the light passing close to it. The gravity associated with the intervening mass acts like a lens, distorting the Point Spread Function (PSF) of the distant light source. The dark matter distribution can be reconstructed over statistical averages of the shapes of millions of background galaxies, which might be distorted by weak lensing. Additionally, by making the measurements on galaxies which are increasingly further away from the observer, characteristics of the galactic expansion

mechanisms can be derived, which has been attributed to the influence of dark energy, thereby extracting dark energy characteristics (Cropper, et al., 2012).

Weak lensing occurs over a very large scale when compared to strong lensing; an example of both effects is given in Figure 2.3 (Mellier, 1999). Strong lensing is visible by eye in the lower left corner of Figure 2.3, but must be averaged over many galaxies for an accurate measurement. As can be seen in the strong lensing example the lensing effect distorts the shapes and relative positions of the galaxies being lensed. However, the weak lensing effect shown in the top right corner and magnified on the right has no distinct pattern visible, this means that weak lensing surveys have to be developed through a statistical analysis over millions of galaxy shapes (Cropper, et al., 2012).

The weak lensing survey will provide maps of the density distributions of dark matter, which cannot be probed directly, to try and determine its role in the Universe. It may be that the theory of gravity needs an additional constant over cosmological scales, or that dark matter is a dynamic field, changing with the evolution of the Universe, such that no constant can be attributed to it (Laurejis, et al., 2012).

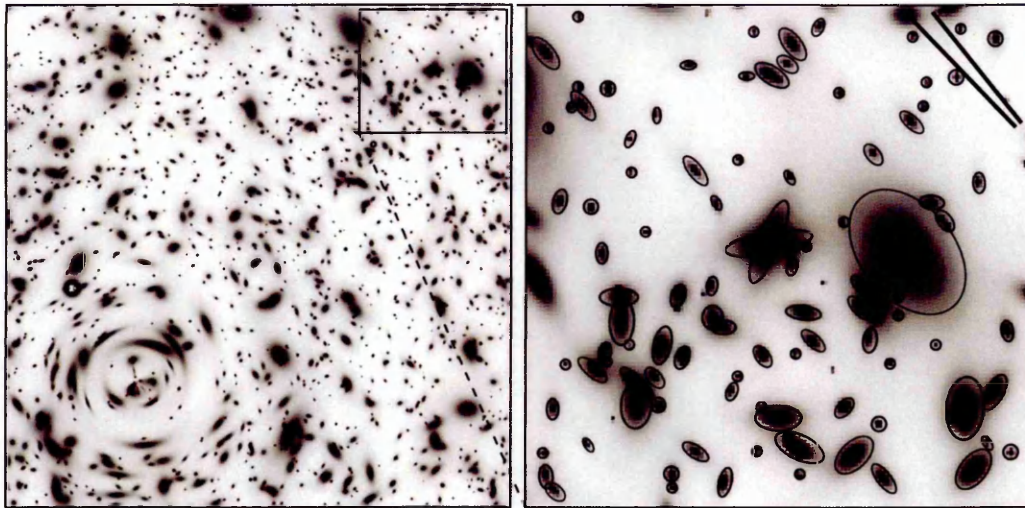


Figure 2.3: Strong and weak lensing regimes shown in a single image. While strong lensing is visible with the naked eye, in the lower left corner, many thousands of galaxy shapes are averaged to provide accurate data about the lensing mass. The weak lensing, visible on the right, requires an average of the shapes of millions of galaxies to produce a map of the large scale structure of the universe (Mellier, 1999)

Space based telescopes, such as Euclid, allow the fine spatial resolution required for the WL survey due to the absence of a turbulent atmosphere experienced on Earth. However, there are several limiting factors to the measured PSF such as imperfections in the optics, several effects in the CCDs used as detectors and space craft “jitter” which may be introduced by the positional mechanisms of the telescope (Cropper, et al., 2012). To allow the recovery of some spatial resolution, the telescope will combine four individual exposures for each image.

2.3.2 The Euclid Spacecraft

Figure 2.4 shows an artist’s impression of the Euclid space telescope that will map a large portion of the sky to an unprecedented accuracy. Euclid will be placed in orbit around the L2 point, which offers a position in space where gravitational forces and orbital motions balance (Amendola, et al., 2012). L2 is approximately 1.5 million km from the Earth and offers a relatively low radiation environment and a stable temperature.

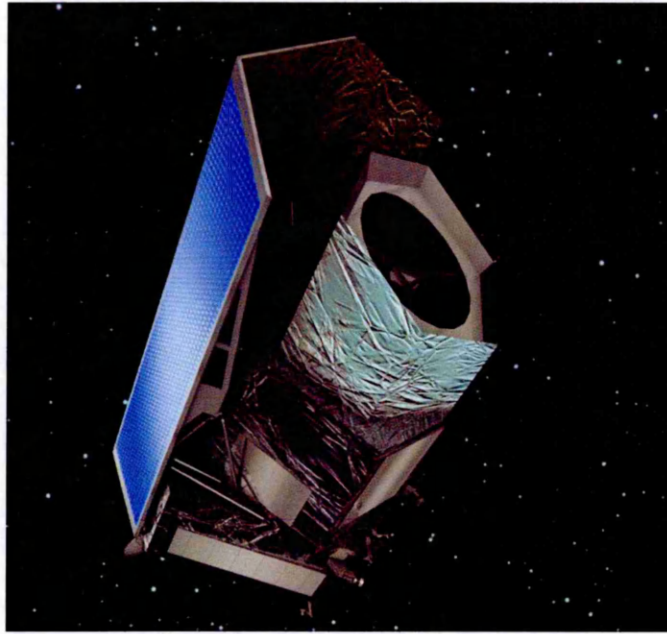


Figure 2.4: Artists impression of the Euclid space telescope, showing the telescope aperture and solar cells. The space craft dimensions are approximately 4.5 m x 1.2 m.

Euclid has a 1.2 m telescope made up of three mirrors with two imaging and one spectroscopic instrument working in the visible and infrared wavelength ranges (Laurejis, et al., 2012). The light incident on the telescope aperture is split into two beams one for each of the VIS and NISP instruments. The VIS CCDs are mounted in the focal plane array, which is currently planned to be made up of 36 closely spaced CCD273s, along with the readout electronics that digitise the data. A schematic of the focal plane can be seen in Figure 2.5 (Cropper, et al., 2012).

2.3.3 The Euclid Focal Plane Array

The focal plane array (FPA) of the VIS instrument has a total area measuring 0.45 x 0.45 m, consisting of an array of 6x6 CCD273s which were designed and manufactured specifically for the Euclid mission. Each CCD has 4000x4000 pixels giving a total number of pixels of the FPA at approximately 600 million. The CCDs are closely spaced, minimising the “dead space” between detectors and giving a >90% fill factor of active silicon (Cropper, et al., 2012), shown in Figure 2.5. Unlike Gaia, the Euclid CCDs will not be windowed around light sources of interest, but fully read out so a detailed survey of a large portion of the sky will be obtained. This will be available to the wider community for auxiliary analysis.

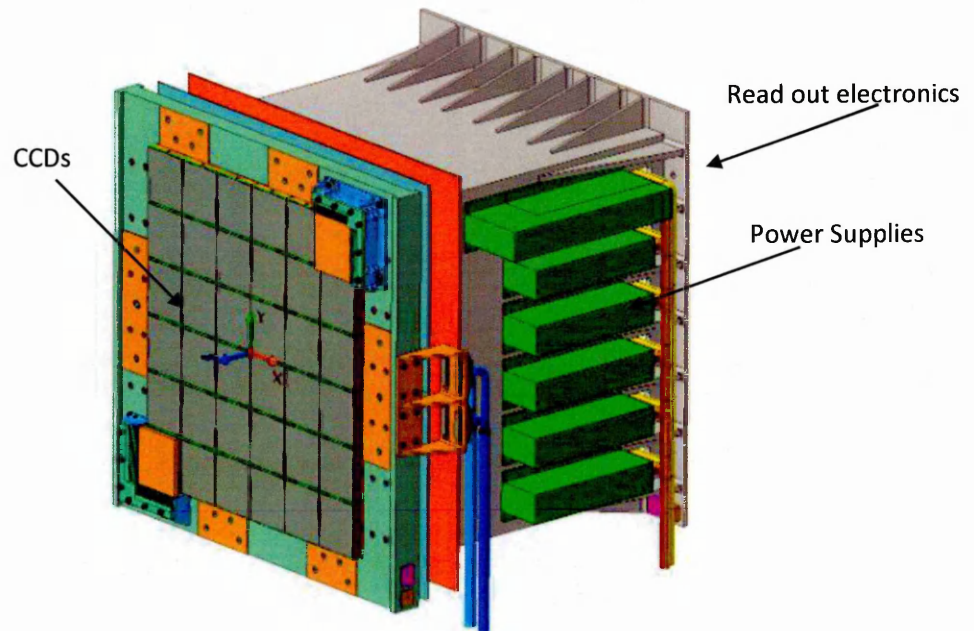


Figure 2.5: A CAD schematic of the Focal Plane Array, FPA, showing the 36 CCD273 detectors mounted on the cold bench and the power supply units for the readout electronics which are mounted inside the module (Cropper, et al., 2012). The focal plane is approximately 0.45 x 0.45 m.

The CCD273, which can be seen in Figure 2.6, was developed for the Euclid mission by e2v technologies Plc. and is the main focus of this thesis. It is manufactured using a four layer polysilicon process, allowing four phase pixels to be manufactured measuring $12 \times 12 \mu\text{m}$. The device is split into two halves by a central charge injection structure which may provide a method for improving Charge Transfer Efficiency, CTE. The serial register has been redesigned from its predecessor the CCD204 to improve serial CTE by confining charge to a smaller volume. The flexible cables, visible in Figure 2.6 were developed to allow close butting between devices on the focal plane, minimising dead space between the detectors.

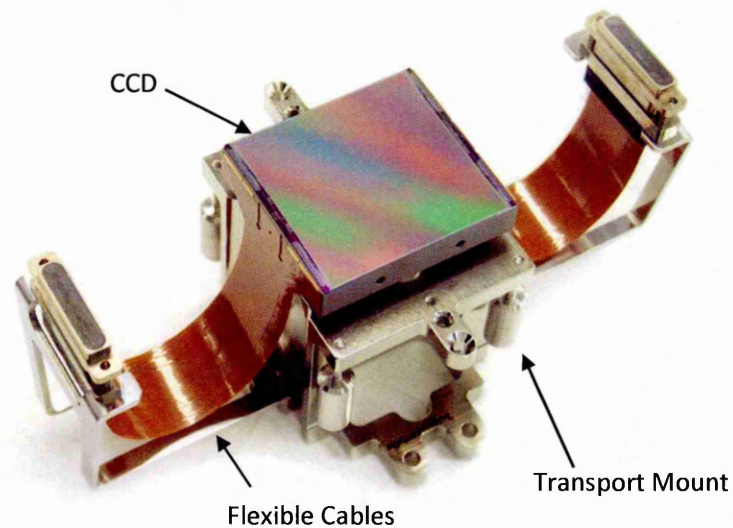


Figure 2.6: Photograph of a Euclid CCD273 test device showing the photosensitive image area and flexible cables, which allow close butting of CCDs in the focal plane array. The CCD area is approximately 5 x 5 cm.

2.4 Radiation Damage Effects in CCDs

The radiation environment both in situ and in transit to L2 is much harsher than that experienced on Earth because it is located outside the protective layer of the Earth's atmosphere and magnetic field. The main concern when considering the space radiation environment are high energy protons which are expelled from the Sun (Cropper, et al., 2012). When a solar proton is incident on a CCD it may cause the displacement of silicon atoms from their lattice positions, leaving empty sections in the lattice known as vacancies, while the displaced silicon atom moves to a non-lattice position, and becomes known as an interstitial atom (Srour, et al., 2003). A large portion of vacancies and interstitial atoms will recombine and have no net effect on the electrical characteristics of the semiconductor, a process known as annealing. In some cases the vacancy and interstitial atom migrate through the structure until they become stable, which can occur through many combinations of vacancies and impurities, or multiple vacancies with examples in Table 2.1. The most problematic vacancy-impurity combination for n-channel CCDs, such as those used in Euclid, is the Phosphorus-Vacancy (PV) centre which occurs when a vacancy combines with a donor phosphorus atom. The PV centres commonly form in the buried channel region which has an abundance of phosphorus atoms, forming electron traps which interact with charge packets and contribute to CTE effects (Pickel, et al., 2003).

A number of common trap types and their properties are listed in Table 2.1 for reference including the Si-E centre (a.k.a. the PV centre), two variations of the di-vacancy (V-V) which is a combination of two vacancies and the Silicon-A centre caused by a vacancy-oxygen combination.

Trap	Energy (eV)	σ (cm ²)	N_t (cm ⁻³)
Si -E	0.46	5×10^{-15}	1×10^{11}
(V-V) ⁻	0.41	5×10^{-16}	1.55×10^{10}
Unknown	0.30	5×10^{-16}	2×10^{10}
(V-V) ⁻⁻	0.21	5×10^{-16}	1.55×10^{10}
Si-A	0.17	1×10^{-14}	2×10^{11}

Table 2.1: Summary of approximate trap properties as commonly referred to in the literature (Hall, et al., 2012) included for reference.

The focus of this thesis is the modelling of the Euclid VIS CCDs to give insight into the radiation effects seen in those CCDs through the way charge is dispersed in the relevant structures during operation. The charge packet characteristics should be directly related to the CTE because charge will only be captured when a trap comes into contact with an electron. As the detectors are exposed to radiation over the mission lifetime, the number of bulk trapping states will increase in proportion to the radiation dose which they receive causing detector efficiency to degrade (Pickel, et al., 2003). The effects of charge trapping can be corrected, by estimating CTE free images using charge capture and release models based on Shockley Read Hall theory described in Section 2.5. An example image showing a corrected star field from the Hubble Space Telescope can be seen in Figure 2.7.

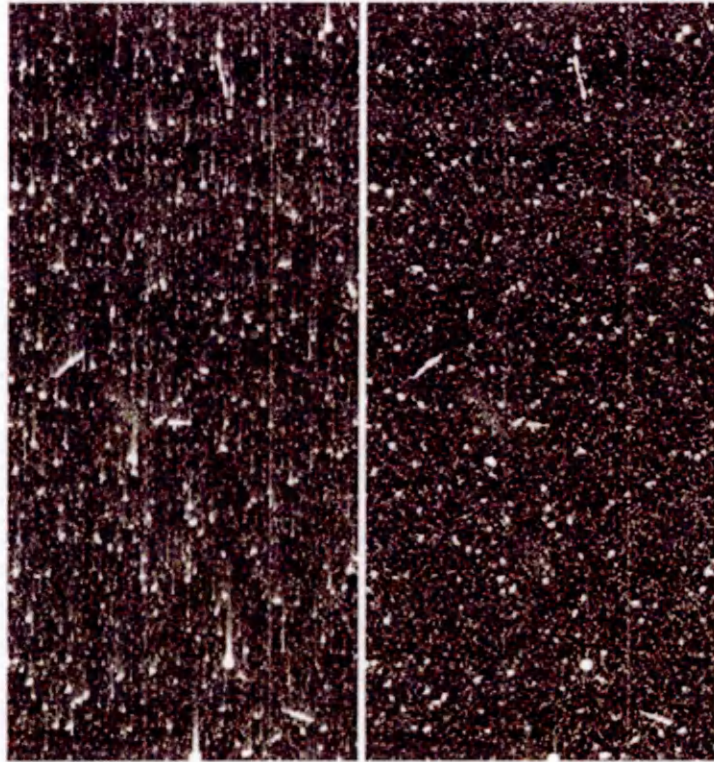


Figure 2.7: This figure from (Massey, 2010), showing a star field captured using the Hubble Space Telescope, with the distorting effects of CTE, left, alongside a corrected version of the same image, right.

CTE distorts the shapes of galaxies in an image, as can be seen in Figure 2.7, this effect is caused by charge trapping and release mechanisms as charge packets move through the CCD. The distortions present in the captured images are very similar to the distortions caused by the weak lensing effect, Figure 2.3, and so must be removed from the images for a reliable weak lensing survey to take place. By improving the understanding of some of the parameters involved in charge collection and storage, the ability to correct these images should be improved.

2.5 Shockley-Read-Hall Trap Theory

Charge Transfer Inefficiency (CTI) in CCDs is caused by the capture and subsequent release of electrons from charge packets as they are transferred through the device. Charge trapping is commonly modelled by Shockley-Read-Hall theory (Shockley & Read, 1952) which describes the probability of capture based on the density of a charge packet which comes into contact with a trap and the amount of time that charge spends in the vicinity of the trap. The capture and emission equations are given below.

In these equations τ_c is the capture time constant of the trap (s), σ is the capture cross-section of the trap (cm^2), n is the density of charge (e^-/cm^2) and v_{th} is the thermal velocity of the charge. Additionally T is the absolute temperature, k is Boltzmann's constant, m_e^* is the effective mass of an electron and t is the dwell time of the charge in each pixel. N_c is the density of states in the conduction band and E is the energy level of the specific trapping state.

$$\tau_c = \frac{1}{\sigma \cdot n \cdot v_{th}} \quad 2.1$$

$$P_c = 1 - \exp(-t/\tau_c) \quad 2.2$$

$$\tau_e = \frac{1}{\sigma \cdot N_c \cdot v_{th}} \exp(E/kT) \quad 2.3$$

$$v_{th} = \sqrt{\frac{3Tk}{m_e^*}} \quad 2.4$$

These equations show that electron capture is dependent on both charge density and the time which the charge packet is in the vicinity of the trap. Emission is determined by the trap properties such as energy level and density, as well as thermal energy available in the device.

2.6 Radiation Damage Mitigation

The effects of radiation damage can be minimised in CCDs through a number of strategies.

Generally the effects of radiation can be reduced through the design of the CCDs or by the way the device is operated. Unfortunately these techniques cannot prevent radiation damage, thus correction techniques are necessary. The following sections describe some common mitigation techniques, particularly those which are used in the Gaia and Euclid missions.

2.6.1 Mitigation through Device Design

In situations where radiation performance is critical, CCDs can be designed with smaller feature sizes, such as narrower transfer registers, which have been shown to improve radiation performance for a given radiation dose. The CCD used in the Gaia focal plane has a large pixel architecture with a $40 \mu\text{m}$ wide transfer channel. However, the Gaia pixel includes a SBC which

confines small signal level charge packets to a reduced transfer channel width. By minimising the channel width, the cross section of the charge packet is reduced at small signal levels this reduces the number of interactions between charge packets and traps to improve radiation performance.

2.6.2 Mitigation through Device Operation

The Shockley-Read-Hall (SRH) equations show that by operating the device at low temperatures and calibrating the charge transfer timings in CCDs, charge can be preferentially emitted into the charge packets from which it was captured, reducing the effects of radiation induced traps and improving CTE (Hall, et al., 2012). These techniques have been successfully used during the calibration and testing phases of the Euclid VIS CCD development to gain optimum CCD performance.

2.7 Charge Packet Modelling

Charge trapping depends on the charge packet coming into contact with a trap. Therefore if the volume that a given charge packet occupies is known, predictions of device performance and the correction techniques can be improved. During the development of the Gaia models and correction techniques, much debate centred around the description of the charge packets collected by the CCD. The models which were developed for the Gaia test campaign are empirically derived from detector testing and fall into two main categories. The charge packet can either be described by the volume driven model or density driven model, which can both be described by the Charge Distortion Model (CDM), Equation 2.5, which is shown graphically in Figure 2.8 (Short, et al., 2012).

$$\frac{V_C}{V_g} = \left(\frac{N_e}{N_f} \right)^\beta \quad 2.5$$

In equation 2.5 V_C is the volume which the charge packet occupies, V_g is the volume of the charge packet at the full-well condition, N_e is the number of electrons in the charge packet, N_f is the number of electrons at full-well capacity and β is a fitting parameter which describes the way charge is distributed depending on signal size.

The charge distortion model describes two possible scenarios, the change in the volume occupied or the change in density of the charge packet as the number of electrons (i.e. the signal level) changes, depending on a fitting parameter β , equation 2.5. The CDM is normalised against signal and volume at FWC, so that the variation in the plot between 0 - 1, Figure 2.8, represents the full signal range.

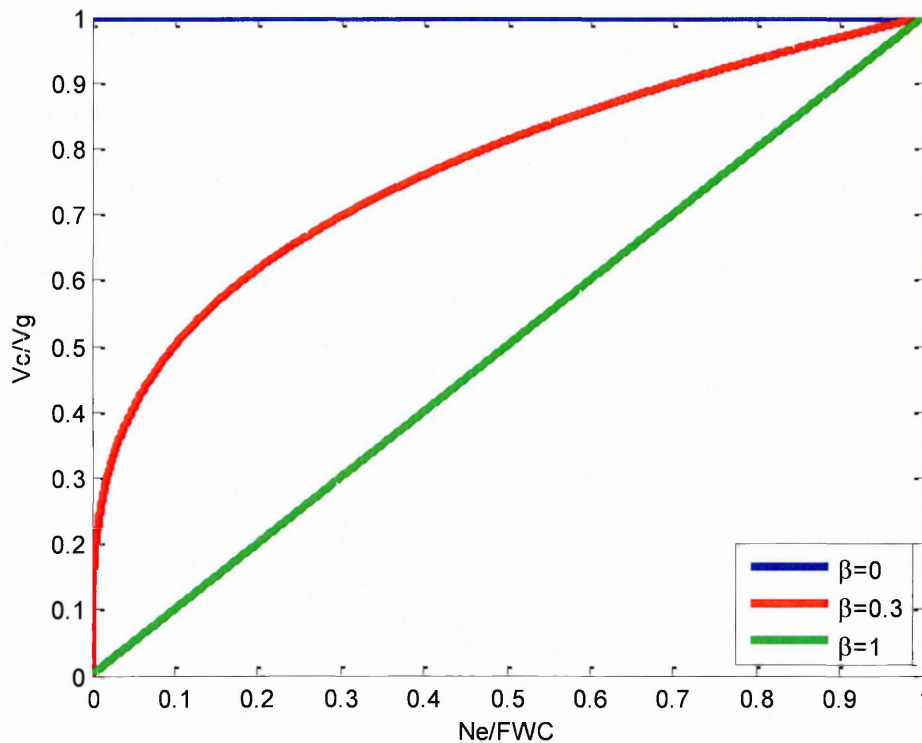


Figure 2.8: ESAs interaction volume function plotted from Equation 2.5. The plot shows the opposing descriptions of constant density and constant volume models (where $\beta=0$ and $\beta=1$). A charge packet where both volume and density change with signal size is described by $0 < \beta < 1$.

In models where $\beta=1$, the volume driven models, the density of electrons in the charge packet is constant and is high enough for trapping to occur instantaneously. Any increase in signal in the charge packet results in an increase in confinement volume, so that density remains constant. Empty traps that occur within the confinement volume will capture charge instantaneously. Assuming that traps are distributed evenly, any increase in trapping will be driven by the change in charge packet volume as signal size increases, hence the volume driven model.

The alternative model, known as the density driven model, where $\beta=0$, describes the charge packet of constant volume where only the density of the charge packet changes with signal size (Short, et al., 2012). As trapping is dependent on the charge density in the vicinity of the trap, according to Equation 2.1, as charge density increases, the likelihood of the trap capturing the charge within the given time period also increases, or conversely, the time period required for electron capture reduces.

Where the fitting parameter is defined between $0<\beta<1$, illustrated in Figure 2.8 where $\beta=0.3$, both the volume and density of the charge packet change with the signal level. This appears to be the most intuitive option when compared against the volume and density driven models.

The interaction volume model was developed through assumptions made about the charge distribution based on experimental observations (Short, et al., 2012). While the Silvaco models presented as part of this thesis make it possible to calculate the electron distribution based on the modelled device parameters and the electrostatic potential fields that confine the charge to the potential wells.

The development of Silvaco models based on physical device structures is necessary because the models described by the charge distortion model do not satisfactorily describe some of the experimental data obtained from Gaia for small signals (Prod'homme, et al., 2011). During the Gaia campaign it was found that exposing the detector to a relatively small background signal had a disproportionately large impact on the measured CTE (Short, et al., 2012). In this case there was an unexpectedly high level of trap occupancy at small signal levels that could not be explained by a charge packet described by this function and is one of the main motivators for the Silvaco work (Prod'homme, et al., 2011).

2.8 Summary

This chapter presented information about recent European orbital telescopes which use CCDs as part of their instrumentation, with some brief references to the HST to give some background to

the detector research that is currently being undertaken. Details about the missions were covered briefly giving an overview of the main instruments and science goals.

The latter half of this chapter gave an introduction to some of the problematic radiation effects that are expected to affect the Euclid and Gaia CCDs, and have been observed in the HST. Ideas that form the foundations of radiation mitigation techniques were introduced along with examples of correction procedures. Finally the concepts behind charge packet modelling are developed as a way to further improve correction algorithms and understand the underlying principles of charge capture and emission, with examples based on work from the Gaia mission development.

Chapter 3: CCD Theory

In 1969 F. Sangster and K. Teer developed an analogue delay line device based on transferring charge between capacitors via pass transistors in a linear array. The device is known as the Bucket Brigade Device (BBD) (Weckler & Buss, 1977) and is still in use in digital signal processing as either a type of analogue memory or a delay line. Their initial idea was modified by W.S. Boyle and G.E. Smith of Bell Labs, who developed the first Charge Coupled Device (CCD) the following year (Boyle & Smith, 1970). The CCD reduced the complexity of the BBD by coupling closely spaced MOS capacitors together, removing the need for pass transistors. By utilising the fringing fields which exist at the edges of capacitors it is possible for charge to move directly between the storage sections of adjacent capacitors, removing any need for control transistors within the charge transfer section.

During their early experiments Boyle and Smith suggested many uses for the new CCD technology, ranging from analogue delay registers to solid state imaging (Boyle & Smith, 1970), it was this suggestion which later earned them a Nobel prize. It is the imaging applications of the CCD, which evolved from these early experiments, on which this thesis is focussed. Even now, more than four decades after their invention, cutting-edge research is still carried out to continue to improve the operational performance and characteristics of CCDs for their use in a wide range of detector applications.

Charge Coupled Devices form the basis of the modern revolution in consumer digital imaging. From their initial commercial use as a replacement for the camera tube in television cameras, their potential for use in scientific applications was quickly realised. The CCD offers much improved imaging performance when compared to other imaging techniques, including size, weight, and power consumption, and considering the improved quantum efficiency over a large range of wavelengths and superior image resolution over the older film and tube technologies.

3.1 Introduction

CCDs are integrated circuit (IC) devices which are manufactured using a specialised MOS process.

A MOS capacitor forms a single element of a CCD array, where an array can be made up of many

thousands of closely spaced MOS capacitors. Charge is not introduced into the device from a source terminal as in MOS transistors and capacitors which are part of standard integrated circuits (ICs). CCDs are photo-sensitive, allowing charge to be photo-generated through photon interactions with electrons in the silicon lattice, referred to as the Photoelectric effect (Sze, 1985). Photons have energy proportional to the frequency of the light which they make up. When a photon interacts with an electron the photon's energy will be absorbed by the electron. If the energy of the electron is then higher than the work function of the surrounding material it is emitted becoming a free carrier and contributes to the electrical characteristics of the material. In CCDs these free charge carriers are integrated into the charge packet. The size of the charge packet is proportional to the intensity of light incident on that area of the detector.

The CCD is made up of a repeating pattern of electrode structures deposited in two, three or four layers and separated by an insulating oxide. The number of layers corresponds to the number of phases, or electrodes, which make up a single pixel in the CCD array. Regions of the device are doped to form channels, within which the buried channel exists to separate charge laterally and hold it away from the surface interface.

Charge is confined in single pixels by the potential barriers created by the "off" (unbiased) MOS gates which are adjacent to the gates biased during image integration. The gates, or phases, which make up the MOS capacitor electrodes extend across the width of the device, where columns are defined by potential barriers, known as channel stop regions, which prevent charge from spreading laterally along the rows. A schematic representation of a section of a typical three phase CCD is shown in Figure 3.9. The term three phase refers to the number of MOS capacitors which make up a single pixel cell.

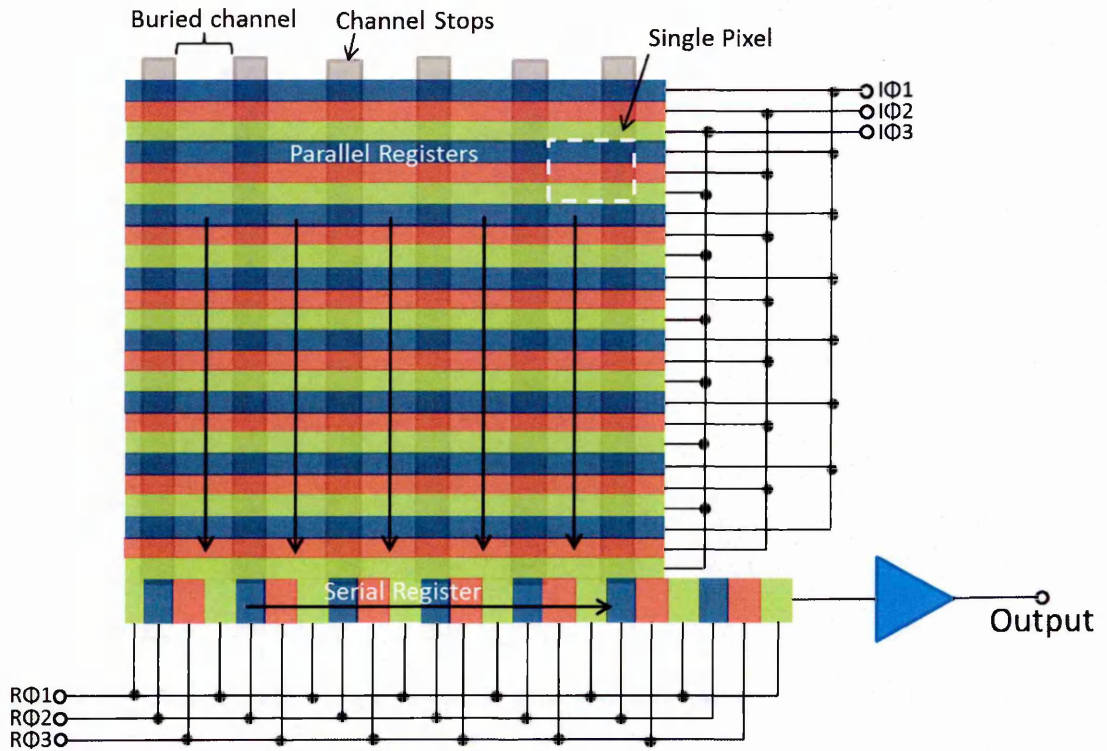


Figure 3.9: A layout schematic of a typical CCD, showing the buried channel, channel stops and gate layout, including labelled clock pulse lines and arrows showing the direction of charge transfer to the output node. In the case of the CCD273 used in Euclid a single pixel is $12 \times 12 \mu\text{m}$ to give an idea of scale.

Once charge has been collected it is “read-out” of the CCD by alternately clocking the closely spaced electrodes which make up the MOS capacitor array. In an ordinary 2D array, there are multiple parallel registers making up the image area which are clocked simultaneously because each electrode extends across the full width of the device. Each of the parallel registers is transferred cell-by-cell into a serial register which is oriented at a right angle to the parallel registers. The serial register is read out completely between line transfers from the parallel registers and is commonly referred to as the readout register. Typically a simple source follower output amplifier is used at the end of the readout register to buffer the voltage signals representing individual charge packets to the off-chip output circuit.

This thesis focusses on the development of semiconductor models to predict the behaviour and evolution of the collected charge packets which are collected in the parallel and serial registers of

the CCD273, which is used in ESAs Euclid Space Telescope. This chapter covers basic device theory, starting from the MOS capacitor, the elementary component of the CCD, to ensure a sound introduction the operating principles of the detectors. An overview of the charge collection and transfer mechanisms is also presented, along with the basic function of the source follower through simplified schematic diagrams, before a review of how all these functions work together to reproduce accurate images.

3.2 Metal Oxide Semiconductor Technology

The title Metal Oxide Semiconductor (MOS) refers to the process technology used to manufacture MOS circuits. The MOS process consists of metal or poly-silicon electrode layers, referred to as the gate, which is separated from the main silicon substrate by a continuous insulating oxide layer, the dielectric, commonly silicon dioxide. CCDs are manufactured using modern MOS process, where the metal layers are replaced with highly doped poly-silicon, which has similar electrical properties to metal. Gate voltage, or bias, is applied to the top layer of poly-silicon, the gate, in the MOS capacitor.

Several poly-silicon layers are used in the manufacture of CCDs, with an individual layer making up every instance of a single electrode phase. Short circuits across adjacent electrodes are avoided by an intervening silicon dioxide layer which surrounds every electrode structure. The silicon dioxide layer acts as an insulator between the electrically conductive poly-silicon electrodes and between the electrodes and doped substrate. However, the presence of oxygen atoms, which can only form two covalent bonds, causes a mismatch in the structures of the two materials, Figure 3.10. This mismatch leaves positively charged 'dangling bonds' or 'interface states' at the surface interface which act to temporarily trap any electrons which come into contact with them.

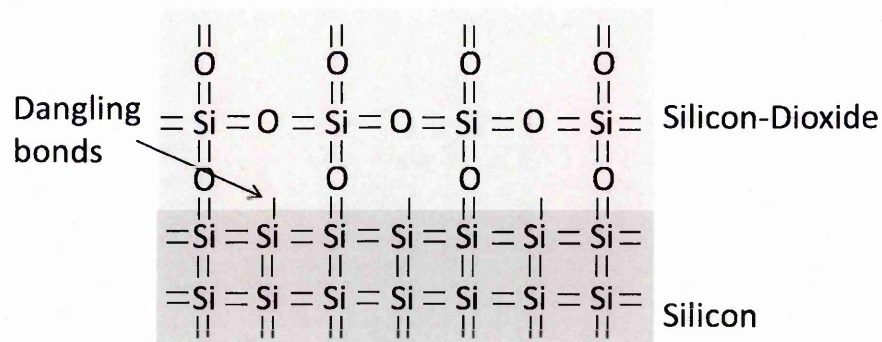


Figure 3.10: Schematic representation of the material bonds at the Si-SiO₂ interface. This shows the mismatch in crystalline structure between the two materials which causes positively charged interface trapping states to form at the surface interface, commonly referred to as dangling bonds.

The trapping sites present at the Si-SiO₂ interface cause problems in many integrated circuit devices. They are one of the sources of 1/f noise in surface channel Metal Oxide Semiconductor Field Effect Transistors (MOSFET) (Janesick, 2007), and they cause a reduction in Charge Transfer Efficiency (CTE) in surface channel CCDs. Thus modern CCDs commonly use a “buried channel” technology, which prevents surface trap interaction under normal operation.

3.2.1 The MOS Capacitor

MOS capacitors are the basic building blocks for many electronic circuits, as they form the gate structures of MOSFETs. Here the focus is on their use in CCD arrays as the collection mechanism for photo-generated charge in part of the pixel structure. Two basic types of MOS capacitor exist, the surface channel and the buried channel device. Although only buried channel devices are used in modern CCDs, both device operations are described to emphasise the advantages of the buried channel structure in the following sections. Figure 3.11 shows the potential diagram of the surface channel MOS capacitors. The buried channel capacitor is shown in Figure 3.12 for comparison.

3.2.2 Surface Channel Capacitor

Assuming the substrate connection is grounded, applying a small positive gate bias to the gate structure of a surface channel MOS capacitor causes a depletion region to form by repelling majority carriers (electrons) from the surface interface. As there are no free charge carriers in a large enough concentration to compensate the voltage applied to the gate electrode, the applied bias is compensated by the fixed dopant ions left behind by the repelled majority carriers. Thus the depletion region width can be set by design, by altering the doping concentration of the substrate. The depletion width can also be manipulated through the bias applied to the MOS gate structure, with larger applied bias resulting in wider depletion regions (Janesick, 2001). Figure 3.11 shows the potential profile when either 0V or 10 V are applied to the electrode of a surface channel capacitor.

Minority carriers which are generated or introduced to the structure are attracted to the high positive potential (the potential well at the surface interface in this case). When the concentration of electrons collected at the surface interface is higher than the bulk substrate doping concentration the device has formed an inversion layer (Sze, 1985). In the case of an n-type enhancement MOSFET or a CCD with a p-type substrate, the inversion layer is made up of electrons, so it acts like n-type silicon and is separated from the p-type substrate by a depletion region. As the charge accumulates at the surface, it acts to compensate the high concentration of fixed ions which form the depletion region, thus shrinking the depletion region and effectively reducing the surface potential. Charge is isolated within this potential well by the barrier of adjacent MOS capacitors with 0V applied to their gates.

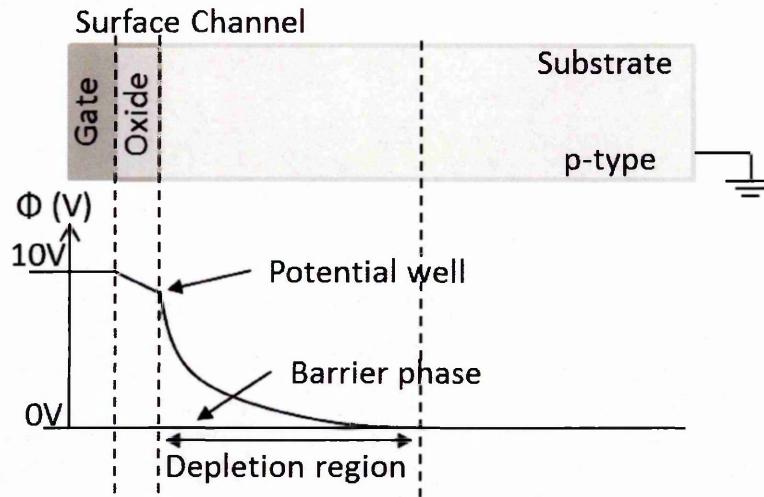


Figure 3.11: Potential well formed in an MOS capacitor in a surface channel device with and without a bias voltage applied to the gate electrode. Charge collects an inversion layer at the oxide-surface interface, attracted by the high potential caused by the bias applied to the gate electrode. Charge is isolated in this potential well in a CCD by the barrier presented by adjacent MOS capacitors with 0V applied to the gate (hence “barrier phase”).

Minority carriers can be introduced through source and drain regions, as in an MOS transistor, or through optical generation of carriers in the semiconductor substrate due to the photoelectric effect. The latter occurs in CCD imaging devices where the only source of the minority charge carriers is thermal generation when the CCD is optically dark. In solid state imaging devices, photo-generated electrons are regarded as useful signal, and thermally generated carriers are a source of noise.

3.2.3 The Buried Channel Capacitor

The basic principle of a buried channel MOS capacitor is to introduce a narrow, highly doped silicon layer adjacent to the Si-SiO₂ surface, which is of the opposite doping polarity to the substrate (commonly n-type doping on a p-type substrate), forming a p-n junction. This causes the high potential to move away from the surface interface to a location within the new highly doped layer, where charge carriers will now collect. Unlike in the surface channel device, this ‘channel potential’ exists even at 0 gate bias, due to the depletion region formed around a p-n junction. The depletion region, and hence the channel potential, is enhanced by the addition of a gate bias (Burt , 1974), as shown in Figure 3.12.

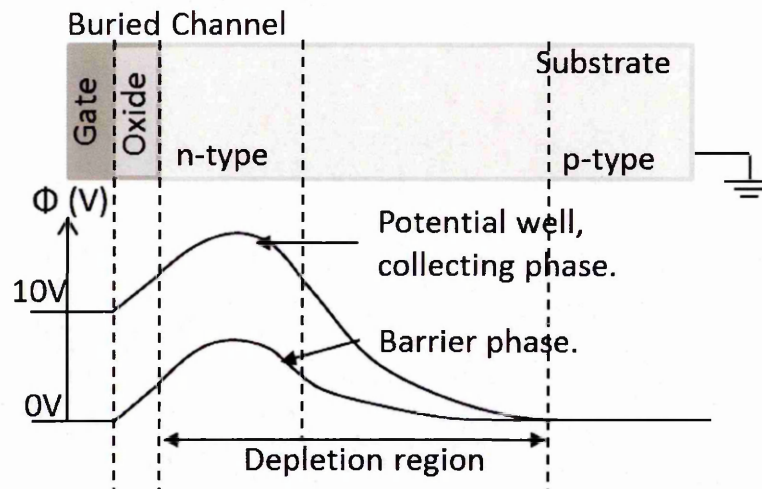


Figure 3.12: Potential profile across the buried channel MOS capacitor. The depletion region around the p-n junction exists without a gate bias voltage. Applying a bias to the gate electrode increases the peak potential and extends the depletion region.

In an unbiased p-n junction, majority carriers from the n-type region diffuse across the junction due to the large carrier concentration gradient, where they recombine with holes in the p-type region. This creates an area on both sides of the junction that is depleted of majority carriers, known as a depletion region. The n-type region in an n-channel CCD is doped such that it is fully depleted of majority charge carriers; therefore it is populated by fixed positively charged ions which cause a potential difference to form across the junction. The maximum potential is located in the n-type side of the junction and is referred to as the channel potential denoted with Φ_{ch} . This is the potential well where charge is collected.

When a positive bias is applied to the gate, the buried p-n junction becomes more reverse biased; this destabilises the equilibrium position by making the n-type side of the junction more positive with respect to the p-type substrate. The depletion region expands so that the fixed dopant ions can compensate the newly applied bias. In general the substrate has a much lower doping concentration than the n-type channel, so the depletion region extends further into the substrate than towards the surface (Figure 3.12).

If charge pairs are photo-generated within the device the electrons will come under the influence of the potential field which is present across the depletion region (Figure 3.13). Electrons will gather at the peak of the potential well, where it is held in a charge packet away from the Si-SiO₂ interface in normal operation. Over the course of single image capture many thousands of electrons can be integrated into a single charge packet. The introduction of negatively charged electrons into the buried channel will act to compensate fixed positively charged ions which create the potential well, thus reducing the peak buried channel potential. The channel moves closer to the interface and at some point the charge will begin to interact with the surface states, this provides a limit to the amount of charge which can be stored in the buried channel.

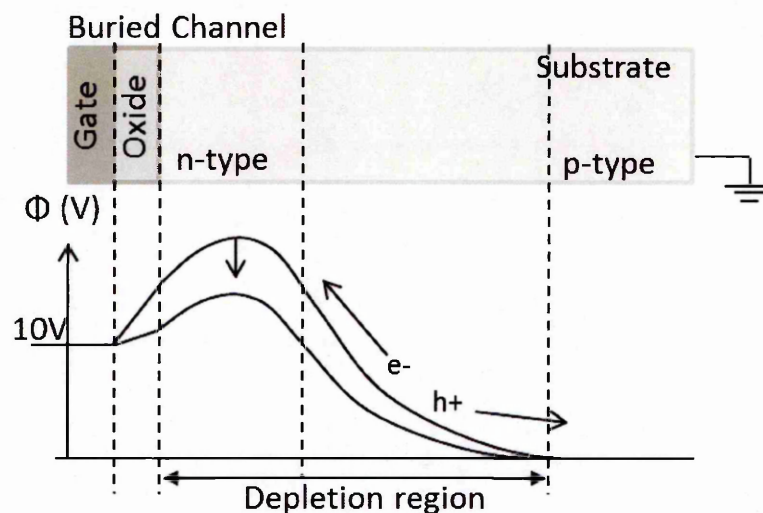


Figure 3.13: Schematic showing the reduction in peak potential and shift in the potential well position associated with charge collection in the buried channel MOS capacitor, which makes up one gate in a CCD pixel. Charge collection within the depletion region is indicated.

The charge collected is isolated into individual pixels because only select gates are biased during charge collection (Figure 3.14). By biasing select gates a potential barrier forms on either side of a potential well, produced by the lower peak potential of the adjacent unbiased MOS capacitor, as shown in Figure 3.12. Charge is isolated laterally due to the presence of 'channel stops', these are areas where the buried channel doping has not been implanted in columns between the parallel

buried channels (in some devices the channel stops are doped p+ silicon to improve isolation). The channel stop regions cause a potential barrier to form which prevents charge spreading laterally, as shown in Figure 3.15. In CCDs the charge collected in any one pixel will be proportional to the light intensity which is incident on the array at that location. By keeping the charge packets separate, the information can be read from the CCD array and an image reproduced.

3.3 CCD Full Well Capacity

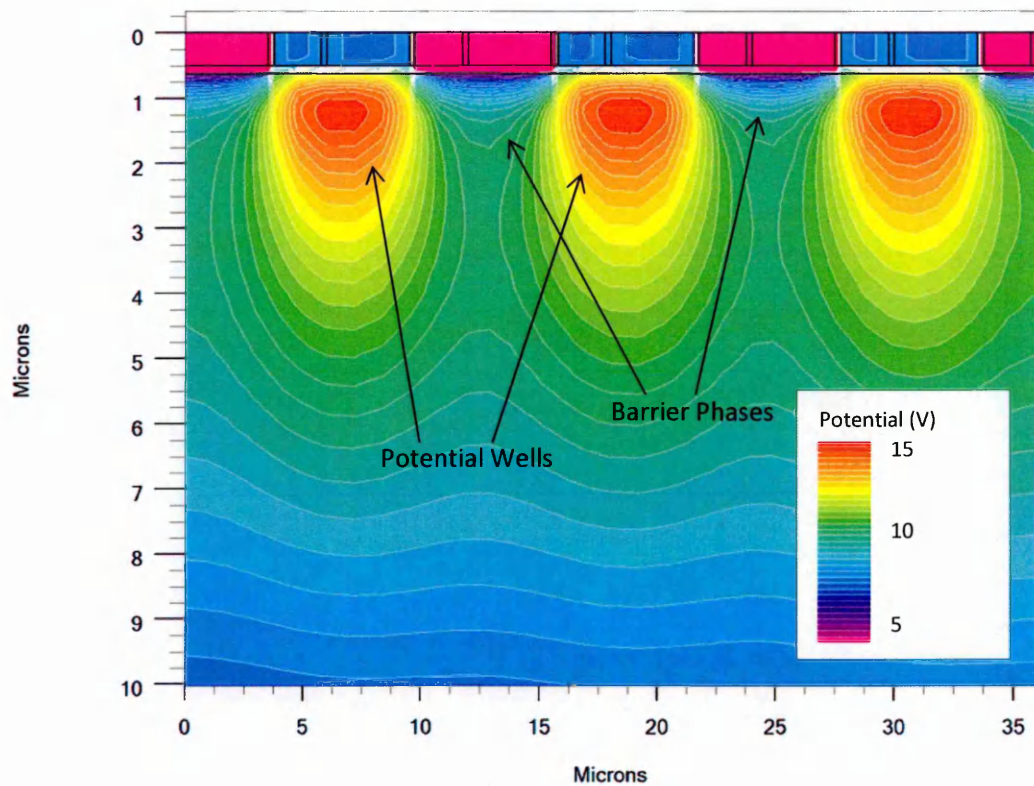
Charge accumulates into discrete “charge packets” within individual pixels where the presence of charge alters the extent of the potential well, proportional to the amount of charge present, (Figure 3.13). Each pixel can only hold a finite amount of charge, a limit known as the Full Well Capacity (FWC), due to the reduction in the potential field and hence the “potential barriers” between pixels, where the potential barrier is the difference in potential between the active potential well and a neighbouring barrier electrode, Figure 3.12. When the potential barrier has been sufficiently reduced the electrons in the charge packet will be attracted to the high potential of a neighbouring pixel, a process known as blooming, which distorts the images of bright objects. When charge moves into neighbouring pixels a saturation limit has been reached known as Blooming Full Well (BFW) (Janesick, 2007).

The potential barrier which separates the charge packet from the surface interface also reduces as charge accumulates. If interaction with the surface occurs, the CTE of the detector will be severely degraded due to interaction with surface states (Figure 3.10). This is known as Surface Full Well (SFW). In either scenario the FWC of the pixel is surpassed. Devices are designed to preferentially bloom under normal operating conditions, preventing the SFW limit from being surpassed, this preserves the CTE of the detector (Janesick, 2007). However operating the CCD with higher gate voltages may cause the SFW limit to be met before blooming occurs, this is discussed in Chapter 6.

3.3 CCD Potential Well Model

Figure 3.14 shows a 2D contour plot of the potential field produced in a CCD register when select gates are biased positive; in this case two adjacent gates are biased at the same time resembling Euclid operation, while the gates adjacent to the actively biased gates are held at a low bias condition. A region of high potential forms beneath the biased gates. This is the potential well, where photo-generated charge is collected during device operation. Charge is confined to the potential wells due to the electric field which is produced by the difference in potential between active and inactive gates. The highest electric field tends to be located at the edges of the potential wells between biased and unbiased gates, or between the potential well and the biased gate where the greatest change in potential is experienced.

Figure 3.14 shows a 2D model of the potential field in three pixels of the Euclid device, running along the transfer channel. Beneath is a schematic of the potential well model, which shows a schematic representation of the change in the potential along the channel. Charge is stored in the areas of high potential indicated by the red areas in the potential well schematic.



Potential Well Model

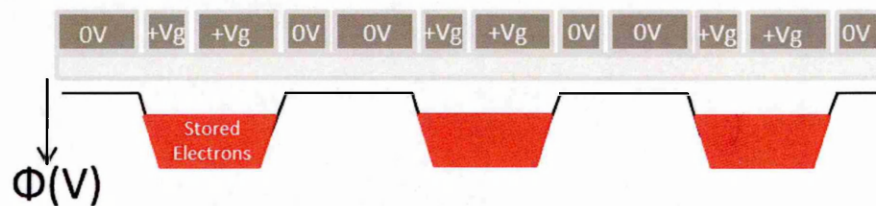


Figure 3.14: Cross section of a four phase CCD register showing the potential wells and adjacent barrier phases as a 2D contour plot, modelled using Silvaco Technology Computer Aided Design (TCAD). In this example, with varying electrode widths resembling the CCD273, there are two adjacent active gates forming the potential well and two barrier phases separating the charge packets. Beneath is the potential well model commonly used to describe the operation of a CCD register.

3.4 Common Pixel architecture

The MOS capacitor forms a basic element in a CCD, where multiple capacitor electrodes (between 2 and 4) form a single pixel. The MOS capacitors exist in a large 2D array which is closely spaced to aid charge transfer. The charge collected by these capacitors is generated optically, through the photoelectric effect and the amount of charge that is collected by each capacitor is defined by the

light intensity incident on that area of the device. The maximum amount of charge that can be collected by any one element is limited by the device doping concentration, gate size and the bias applied to the collecting element, as well as the oxide material and thickness and is referred to as the Full Well Capacity (FWC).

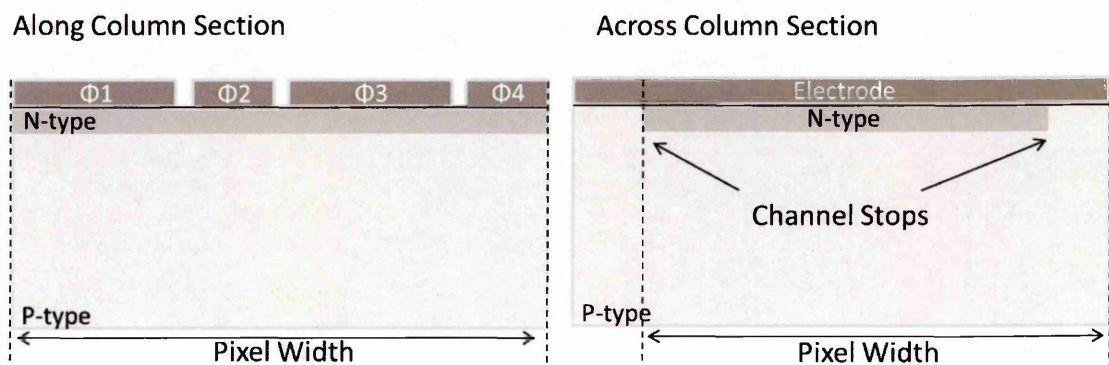


Figure 3.15: Cross-sections in two dimensions (across and along the buried channel) giving an example of a typical pixel architecture, showing the buried channel, channel stops and gate depositions in two cross sectional views.

Figure 3.15 shows a schematic representation of a single pixel showing the major architectural components which make up a CCD pixel. CCDs are primarily used to collect and store photo-generated charge from a large range of light wavelengths. The photoelectric effect causes incident light to generate electron-hole pairs from weakly bound valence electrons that are excited into the conduction band, leaving behind a hole in the valence band. Higher energy photons can produce multiple electron-hole pairs. Where the energetic conduction band electron collides with other valence electrons (Janesick, 2007) the amount of charge generated can be related to the energy of the incident photon.

3.5 Device Architecture and Charge Transfer

Once charge is collected and confined to individual pixels in the image area of the CCD, information which it represents must be “read out” and measured. This is achieved through the charge transfer mechanism, where charge is moved from electrode to electrode along a register. Charge transfer is done in each of the parallel registers at the same time, to move one row of

charge into the serial register. The serial register is read-out fully before another row of charge is moved into it from the parallel registers. A schematic of a simple CCD architecture is given in Figure 3.9, along with arrows indicating the charge packet readout path. Charge is moved along to the output node, where it is converted to a voltage value proportional to the charge level of the specific pixel being read, through the use of a reset capacitor (C_n) and a source follower output amplifier as described in Section 3.7.

Taking a three phase device as an example, as in Figure 3.9 and Figure 3.16, each MOS gate within a pixel is referred to as a phase (Φ_1, Φ_2 etc.). The same phase in each pixel is connected to the same clock line and is manufactured in the same poly-silicon layer. Charge is collected beneath the integrating phase - in Figure 3.16 this is Φ_2 . Once charge has been collected, the adjacent phase (Φ_3) is biased positive, to the same voltage value as Φ_2 . This causes the charge packet to drift laterally under the influence of a potential gradient. The charge packet is now shared between both active gates. Next the originally integrating phase Φ_2 'turns off' (the voltage is reduced to that of the other inactive electrodes), and as this gate is turned off, charge is once again moved under the influence of the electric field into the high potential gate, now Φ_3 , where all of the signal charge for that pixel is confined. This process is repeated between the adjacent MOS electrodes that make up the register until the charge moves to the starting phase (Φ_2) in the next pixel along the register. There is a barrier between pixels at all times during this transfer process produced by the unbiased phases, to maintain image resolution (Figure 3.16).

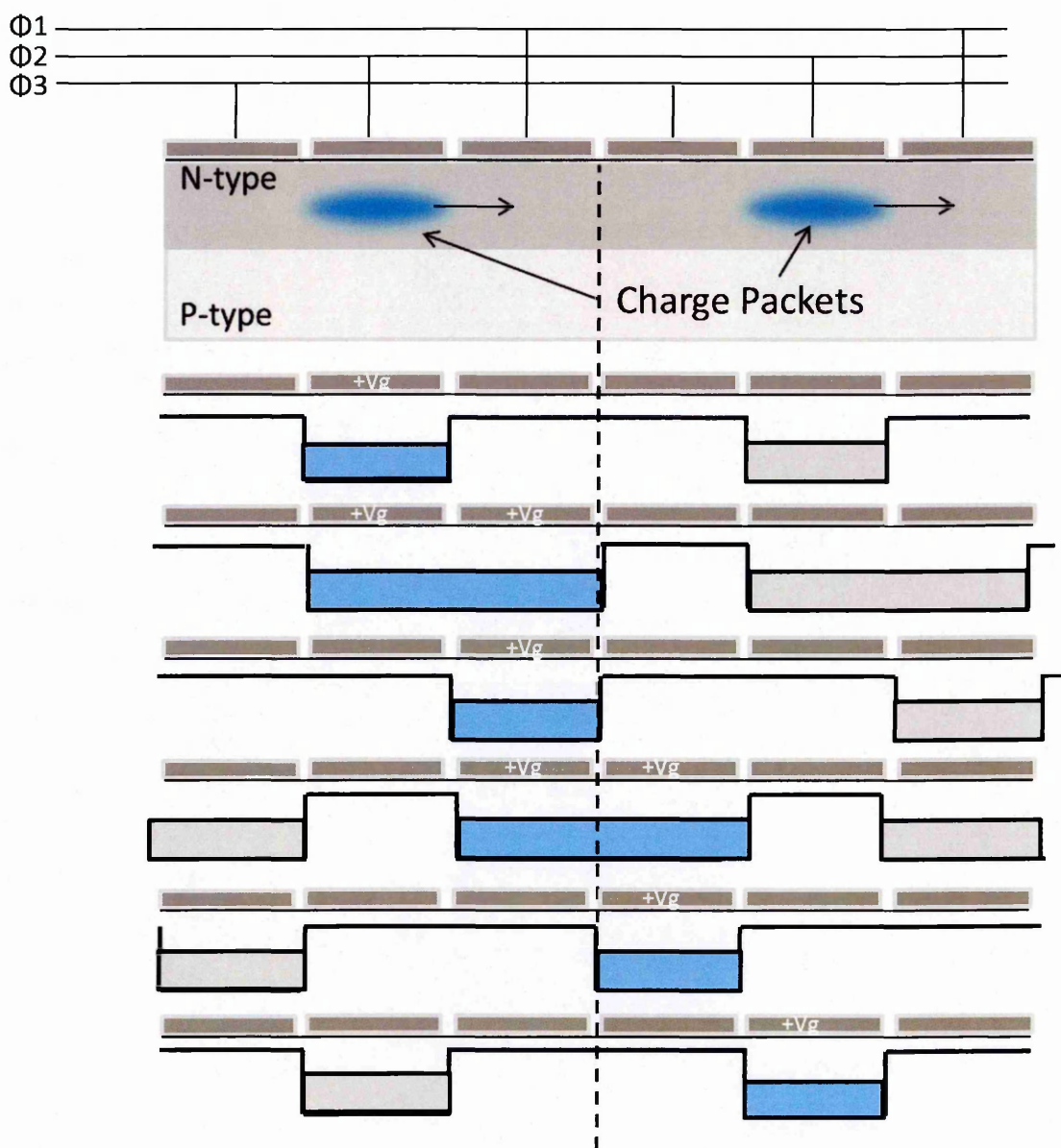


Figure 3.16: Schematic of the charge transfer process in two pixels of a three phase CCD register. This process occurs across all parallel registers simultaneously to transfer one row into the serial register, the serial register is then read out fully before the next row of charge is transferred from the parallel registers.

The readout sequence described in the last paragraph, and shown schematically in Figure 3.16, is just one of many possible readout sequences. Other sequences are described in chapter 6 which were used during device testing.

In some cases a very small fraction of the charge will be left behind at each transfer and will arrive at the output later than the charge packet from which it originated. This makes the charge

transfer efficiency (CTE) an important measure of device performance. Poor CTE may be attributed to the presence of bulk trapping states, an inefficient clocking sequence, or a large inter electrode gap.

3.6 Charge Transfer Efficiency

Charge Transfer Efficiency (CTE) is defined by the proportion of charge which is successfully transferred between two pixel elements (Burt , 1974). As such it varies depending on the signal size of the charge packet undergoing transfer and the operating parameters which control the transfer, such as applied bias voltages and switching speed between adjacent gates. Assuming optimised operating parameters and device layout, the main contributing factor to charge loss during transfer are lattice defects, which act to trap charge by introducing intermediate energy levels in the silicon band-gap. Charge traps come in several common configurations which have unique trapping properties (Srour, et al., 2003) (Hopkinson, et al., 1996).

CTE is defined as the proportion of the charge packet which is successfully transferred during the transfer between elements and can be upwards of 99.999%. For convenience the inverse term, charge transfer inefficiency (CTI) is often used, where $CTI = 1 - CTE$, and is usually in the range of 1×10^{-5} for scientific CCDs. Transfer inefficiency is a cumulative effect, since it is applied at each successive charge transfer. Thus the charge loss from each charge packet increases with the number of transfers. Transfer efficiency is an important parameter especially in large area CCDs where charge packets may undergo thousands of transfers, meaning even a small inefficiency can cause unacceptable charge loss.

Charge trapping is a major problem in surface channel devices, where the concentration of surface traps is high when compared to bulk traps, and charge is transferred in a narrow layer along the surface interface. If a trap comes into contact with the charge packet a small portion of the charge may be trapped and re-emitted later into a trailing charge packet, where trapping time constants depend on the trap properties and device temperature according to Shockley-Read-Hall trapping theory (Shockley & Read , 1952) (Hall, et al., 2012).

It is possible to improve transfer efficiency through both device design and operation. Closer spacing between adjacent gate elements can increase the effect of fringing fields between gates and improve the transfer between individual electrodes. It is also possible to reduce the clock frequency during charge transfer; however, a lower speed limit is defined by the thermal charge generation inherent in semiconductor devices.

3.7 CCD Output Circuit

Charge collection, storage and transfer are arguably the most important aspects of CCD operation, but converting the information collected into a useful form for further processing or storage off-chip is also an important factor in device operation. The task of converting charge packets to useful voltage signals is achieved through the operation of the output amplifier, which is made up of a number of Metal Oxide Semiconductor Field Effect Transistors, or MOSFETS.

The voltages that are generated are sent “off-chip” to be further amplified and converted to digital signals using an Analogue-to-Digital Converter (ADC), which is external from the CCD package. Figure 3.17 shows a microscope image of the sense node and output amplifier from a Euclid CCD273 device; this is a top down view of the circuit layout, which is recreated as a schematic in Figure 3.18 for convenience.

drain terminals. By applying a voltage bias to the gate terminal the flow of charge between source and drain can be controlled (Sze, 1985).

The output amplifier is located at the end of the serial register (Figure 3.17) and is the method by which the analogue charge signal is converted into a useful voltage signal. Under normal operating conditions, the voltage across the output node capacitance (C_n) is set to a known level (V_{ref}) by applying a gate bias pulse (Φ_R) to the reset transistor. After the reset pulse the node is disconnected from V_{ref} and left floating until the current charge packet (Q_n) is transferred from the serial register across the output gate (OG) to C_n . The presence of the negatively charged electrons which make up the charge packet change the node voltage proportional to the number of charge carriers present in the charge packet, according to $V_{cn}=Q_n/C_n$ where C_n is a constant set at the time of manufacture. C_n is the sum of all the parasitic capacitances at the output node.

Charge is transferred one packet at a time from the serial register onto the output (sense) node, represented by C_n in Figure 3.18, after it has been reset to V_{ref} . The CCD is designed so that sense node capacitance is very small, as the charge on the output node, C_n , produces a voltage drop across the input of a source-follower amplifier. The voltage drop across the source-follower input is proportional to the charge on the sense node and inversely proportional to the capacitance of the sense node according to $V_{cn}=Q_n/C_n$, therefore making C_n small boosts the input voltage. The output voltage from the source follower is found to be proportional to the input voltage (Equation 3.6).

$$V_o = V_i - V_T - \sqrt{\frac{2I_D}{\beta}} \quad \therefore V_o \propto V_i \quad (V) \quad 3.6$$

The source follower operates in the manner described by Equation 3.6 because the output transistor is held in saturation mode, where saturation is defined by the ratio of V_{DS} : $V_{GS}-V_T$, when $V_{DS} > V_{GS}-V_T$. Where V_{DS} is the drain-source voltage across the transistor, V_{GS} is the gate- source voltage across the transistor and V_T is the threshold voltage of the transistor. This condition

occurs in the source-follower circuit because $V_{DS}=V_{od}-V_O$ and $V_{GS}=V_i - V_O$ in the output transistor, as V_i cannot exceed V_{od} , then $V_{DS} > V_{GS}-V_T$ is satisfied (Figure 3.18).

The final output voltage which is sent “off-chip” is determined by the gain of the source-follower amplifier, A_{SF} , where $A_{SF}=V_O \times V_{Cn}$. V_{Cn} is the voltage drop across the sense node capacitance and hence is the input voltage of the source-follower, which has been derived, therefore the final V_o voltage can be determined by Equation 3.7:

$$V_o = A_{SF} \times \frac{Q_n}{C_n} \quad 3.7$$

The output amplifier is governed by a parameter known as responsivity, which is the voltage change caused by a single electron on the sense node. Equation 3.7 shows responsivity to be ultimately governed by the capacitance of the sense node. Therefore it is made as small as possible to keep the responsivity at a reasonable level.

The readout process and conversion from an analogue charge to a signal voltage, which can be converted into a digital number (DN) by an off-chip ADC, for use in a computer system, is performed for each individual charge packet. In larger CCDs with many thousands of columns and rows, the readout process can take a long time (10ms Vs 10 μ s) in comparison to the time it takes to transfer a single charge packet from one pixel to the next. Many modern large area CCDs are separated into sections, where each section will have an individual readout register and amplifier. However multiple output amplifiers can introduce extra sources of noise to measurements because of the different voltage offsets and manufacturing variability present in the transistors which make up each of the amplifiers.

3.7.1 Multi Stage Amplifiers

Additional stages on the output amplifier are common in modern scientific CCDs. The Euclid CCD273 and the CCD204, which are discussed extensively in this thesis, both use a two-stage amplifier. The basic principles are the same as the single stage amplifier covered in the previous section. A second stage will share a similar architecture with the first, including a floating

“diffusion”, which acts as a capacitor, connected to a reset reference voltage through a reset transistor and an output amplifier. A schematic can be seen in Figure 3.19.

The second stage of the amplifier acts to lower the output impedance of the device, which reduces the time period associated with the output load voltage swing, allowing readout to be performed at a higher rate (Janesick, 2007). The reduction in output impedance is achieved by increasing the width of the second stage output MOSFET, which reduces the source/drain impedance of this transistor and increases the current capacity of the second stage output. This architecture can be seen in Figure 3.20.

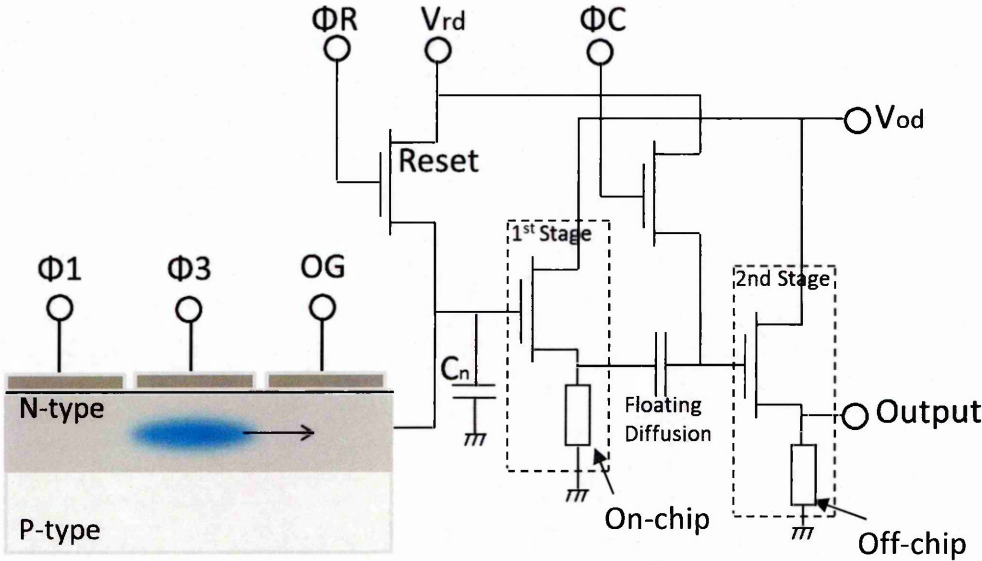


Figure 3.19: Schematic representation of the two-stage amplifier used in the CCD273 and CCD204. This introduces an extra floating diffusion capacitor at the input to a source follower amplifier. The second stage amplifier is similar to the first stage, but with increased current capacity provided by wider transistors.

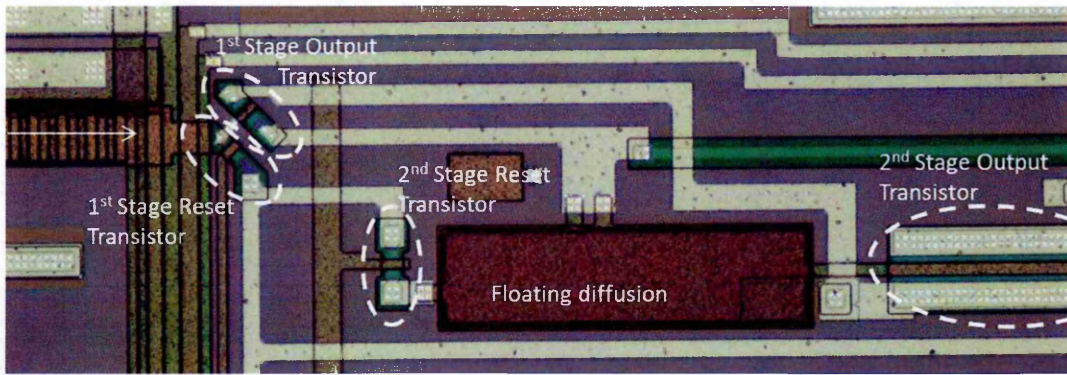


Figure 3.20: Microscope image of the two stage amplifier on the CCD273. Notice the size of the 2nd stage output transistor compared to the 1st stage, enabling a higher current capacity.

3.8 CCD Noise Sources

All electronic circuits have noise sources that cause a random fluctuation in a given electrical signal. CCDs are no exception; here a brief introduction is given for several common sources of noise in a CCD camera.

3.8.1 Reset Noise

Reset noise is experienced in the output circuit of the CCD and describes a variation in the reset level of the output node. It is usually described under the wider title of read noise. Reset noise is attributed to the small resistance experienced in the conducting channel of the reset transistor (Janesick, 2007) and is therefore associated with thermal noise. Ideally the reset operation would set the sense node voltage to exactly V_{REF} but a fluctuation will occur in the reset level between output pulses when the node is left floating at the reference voltage.

3.8.2 Read Noise

The output amplifier is itself a source of noise which is the first noise source added to the voltage signal in the readout chain. There are several types of noise which can be associated with the output electronics and these include 1/f noise produced when charge moves through transistor channels (Sze, 1985), reset noise due to the variation of the reset level applied to the sense node and thermal noise caused by the various sources of resistance in the output electronics. These cumulatively make up the read noise, which is added to the signal voltage generated from each

individual charge packet (Janesick, 2007). Read noise is an important parameter because it sets the lower limit for the useful detection of signal.

3.8.3 Quantisation Noise

The signal output from the output amplifier is further amplified off-chip and converted to a digital number (DN) through an analogue-to-digital converter (ADC). The accuracy of the digital number as a representation of the voltage level depends on the ADC circuit, where a typical 14-bit ADC will resolve a value down to 16384 levels of quantisation. The error associated with analogue conversion resolution represents one source of noise on the signal output. The process of conversion resolution represents one source of noise on the signal output. The process of analogue-to-digital conversion makes it possible to store and process the information read out of the CCD in a digital computer system.

3.8.4 Thermally Generated Dark Current

Dark current is unwanted charge that is collected by the potential wells of the CCD due to the random thermal generation of carriers inherent in semiconductor devices. These thermally generated charge carriers are indistinguishable from the useful signal, so this process makes a major contribution to the system noise experienced in semiconductor devices. It is so called, because thermal generation will occur continuously, even when no light is incident on the CCD. Crystallographic imperfections with and without association of common impurities, can introduce new energy levels within the silicon band gap, Figure 3.21 and Figure 3.22, and these can act as generation-recombination centres, or 'traps'.

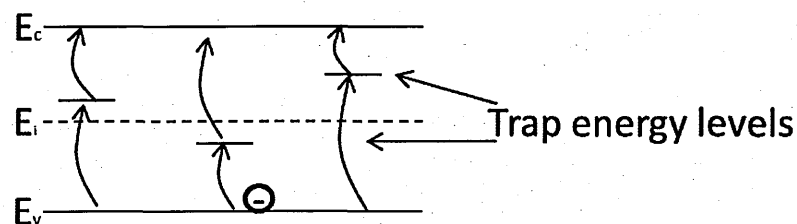


Figure 3.21: Silicon band gap showing the extra energy levels introduced by a trap site in the bulk silicon substrate.

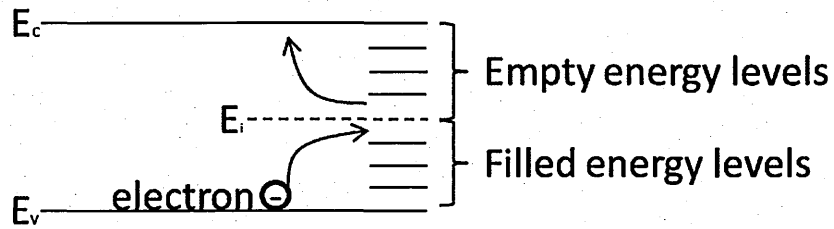


Figure 3.22: Silicon band gap showing the extra energy levels introduced by a trap site at the surface interface. These extra trap sites increase the probability of charge carriers gaining enough energy to transition between the valence and conduction bands.

Most of the bulk traps are found in the centre of the silicon band-gap, close to the intrinsic, mid-gap energy level E_i (Figure 3.21). As the energy level of the trap moves away from E_i , the probability of generation/recombination reduces exponentially (Srour, et al., 2003). The extra energy levels thus introduced act as an intermediate level for electrons transitioning between the valence and conduction bands. In this way the extra energy levels in the silicon band-gap act to increase the probability of charge carriers gathering enough thermal energy to transition from the valence band to the conduction band.

Figure 3.10 has previously shown the silicon lattice is mismatched at the interface with the insulating silicon oxide. This constitutes the largest lattice defect site within an MOS device. Regularly arranged “dangling bonds”, or interface traps, have the same effect on the silicon band-gap as described for bulk defects (Figure 3.22). As such the surface trap sites can form the largest contributor to dark current generation (Janesick, 2007).

In many scientific applications the effects of dark current can be reduced by cooling the imaging array, where the amount of cooling necessary is dependent on the integration time needed to give a reasonable signal to noise ratio for the application. It is possible to further reduce dark signal generation by increasing the readout rate.

3.9 CCDs Used In This Study

3.9.1 The e2v CCD204

The CCD204 was developed by e2v technologies for use in astronomy as a broadband (broad wavelength) photometric imager (e2v Technologies, 2008). It was used as a base design for the development of the CCD273, which will be used in the Euclid mission. The CCD204 is a full frame, large image area device with 4096×1064 pixels read out through two output amplifiers.

The CCD204 device is manufactured on “deep-depletion” silicon, which is back-thinned. This gives high quantum efficiency and sensitivity (e2v Technologies, 2008). The image area is made up of pixels that are $12 \times 12 \mu\text{m}$, while serial register elements are $12 \times 50 \mu\text{m}$ allowing charge binning up to 2×2 pixels. Readout noise is minimised through the use of two-stage output amplifiers with dummy output circuits allowing common mode rejection. This improves the sensitivity of the device for low noise applications. There is also an injection structure which is located at the top of the image section which allows the injection of a known amount of charge into the image area row-by-row.

3.9.2 The e2v CCD273

The CCD273 follows much of the same design criteria as the CCD204 on which it is based. It is a full frame, deep depletion, large area device with $12 \times 12 \mu\text{m}$ pixels. The serial register differs from the CCD204, with only a $20 \mu\text{m}$ channel width. This reduces the serial Full Well Capacity (FWC), but should improve radiation performance. The CCD273 is larger overall, with 4096×4096 pixels, readout is achieved through 4 output amplifiers, with the device split into quadrants with an injection drain separating the top and bottom halves of the image section.

3.9 Summary

This chapter has discussed the basic formation, structure and operation of a typical CCD, with examples of common features and device architecture. Starting from the simplest element of a CCD, the MOS capacitor, descriptions of earlier surface channel devices have led to the formation of modern buried channel device theory and the relative improvements made. The charge transfer mechanism was discussed along with a description of the CTI phenomenon and variables which may prevent efficient detector operation. A schematic description of the sense node

operation and output amplifier have also been made with reference to the amplifier operation and expected operational performance using circuit analysis. Descriptions of common noise sources have also been given; this introduces some of the concepts concerning noise measurements made in later chapters. The final section of this chapter gives technical details of the detectors modelled and used in later chapters.

Chapter 4: CCD Modelling Techniques and Measurements

Semiconductor manufacturers can predict many aspects of device functionality using a combination of sophisticated design software suites and rules of thumb based on many years of empirical results and experience. This thesis is partly aimed at developing an understanding around current assumptions of device functionality during the design and development stages for CCDs, and further expanding existing predictive methods and device knowledge. This work is strongly driven by the Euclid VIS instrument and the intricate device knowledge needed to produce data of a very high accuracy to meet mission targets. This chapter will focus on the development of the Silvaco TCAD device models and the methods used to interpret the results. Later chapters discuss the results and how they can be used to determine device performance.

Silvaco TCAD is a semiconductor device simulator used in both industry and academia. It can be used to predict electrical, thermal and optical behaviour of semiconductor devices from a user specified device structure, doping and bias conditions (Silvaco Inc., 2010). By directly applying Poisson's equation and accepted carrier models it is possible to predict device functionality and parameters that are difficult or impossible to measure directly, such as charge distribution within the structure. Parameters that can be measured directly are used to verify device models and are based around potential and FWC measurements; this work is presented in later chapters as well as an analysis based on CTI measurements.

4.1 Silvaco Model Development

Silvaco is a specialised TCAD software package designed specifically for semiconductor modelling. Models are produced in the Silvaco ATLAS module and are based on the device design dimensions and materials. The device dimensions in the models are derived from CAD schematics provided by e2v (private communication). The Silvaco software predicts the electrical behaviour based on the specified physical structure, biasing conditions and device doping which is achieved through the application of sets of discretised differential equations, based on Maxwell's laws, onto a user specified two or three dimensional grid which represents the modelled structure. Silvaco also

enables the simulation of charge carriers in the models through the application of continuity and charge transport equations (Silvaco Inc., 2010).

4.1.1 Model Mesh Definition

The mesh, specified by the user, is an important part of designing a new model. It is the first section of the input deck to be interpreted and sets the ground work for the device simulation. Solutions to the semiconductor equations are derived for each node point in the mesh, or in the case of a vector value, along the mesh lines. Therefore a coarser mesh results in faster simulation times, and a finer mesh results in increased accuracy but is computationally expensive.

In most cases it is possible to vary the density of the mesh over the device area. In the case of the CCD simulations a fine mesh is defined for the polysilicon electrodes, oxide and the top $\sim 5\mu\text{m}$ of the silicon substrate. These areas are chosen because charge packets and the electrical behaviour around the buried channel are of highest interest. Beyond these areas a coarser mesh is used as only approximate values are necessary to aid convergence in the simulation solution and maintain a balance between accuracy and simulation speed (Figure 4.23). The main area of interest in these models is the buried channel, which lies at a depth of $\sim 2\mu\text{m}$, and the surface interface between the silicon substrate and insulating oxide at $0.56\mu\text{m}$. A dense mesh in these areas will give accurate information about charge collection and will provide good accuracy for charge packet models.

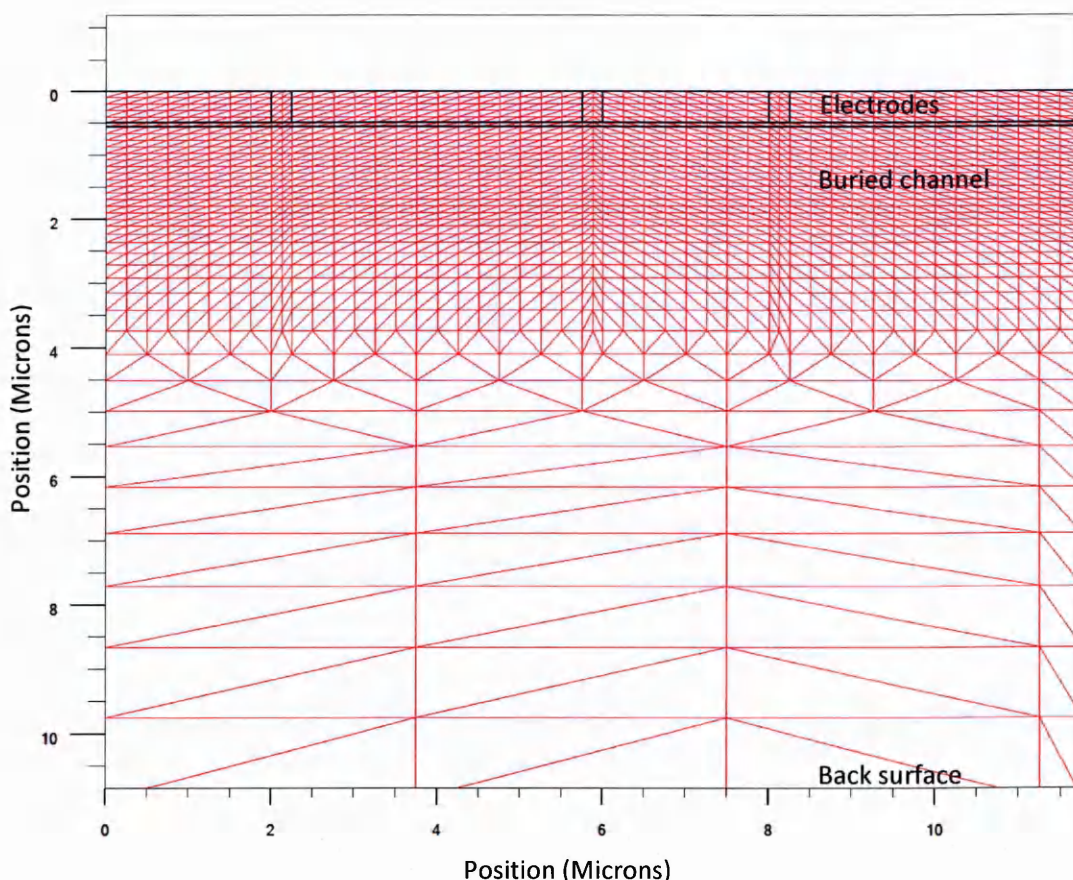


Figure 4.23: A typical device mesh from a CCD273 pixel simulation showing a finer mesh in the areas of interest (where rapid changes in voltage or doping are expected), these generally occur close to the surface interface. Coarser mesh is used in areas of lower interest to maintain simulation time.

A simple 2D model of the Euclid pixel is used to demonstrate the effect of the mesh on both simulation time and the accuracy of the resulting data. The same structural geometry is used in each simulation, with the only changes occurring in the mesh spacing in the lateral, x-dimension, between simulations. Due to the need to have mesh points at material junctions, doping junctions and structural changes, the mesh is automatically calculated between these positions and therefore may not be precisely spaced across the entire model, but spacing between these points are exactly as described, as can be seen in Figure 4.23.

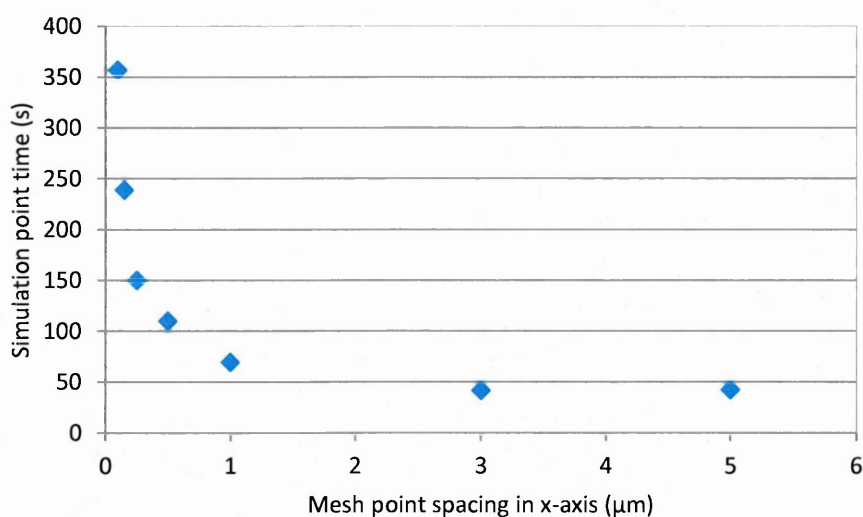


Figure 4.24: Change in simulation time depending on mesh spacing along the x-axis, using a mesh in a simple 2D Euclid pixel model. The graph shows an exponential decrease in simulation time as the distance between mesh points increases.

The mesh spacing in the x-dimension is varied between 0.1 and 5 μm , with the output simulation time recorded for each mesh solution. This information is displayed in Figure 4.24, which shows an exponential increase in simulation time as the mesh density increases. Mesh distributions as coarse as 3 and 5 μm would never realistically be considered for this device because they are much larger than the feature sizes of the model.

The various mesh distributions can also be compared against the resulting device data from the solved model. Figure 4.25 shows a large difference in the model output depending solely on the mesh layout; in this example the peak value of the potential well is examined. As the mesh tends towards the much denser layouts only small changes in the simulation output is achieved. Figure 4.26 quantifies the difference in the potential measured at the peak of the potential well of Figure 4.25, as a percentage difference when compared to the value measured from the densest mesh.

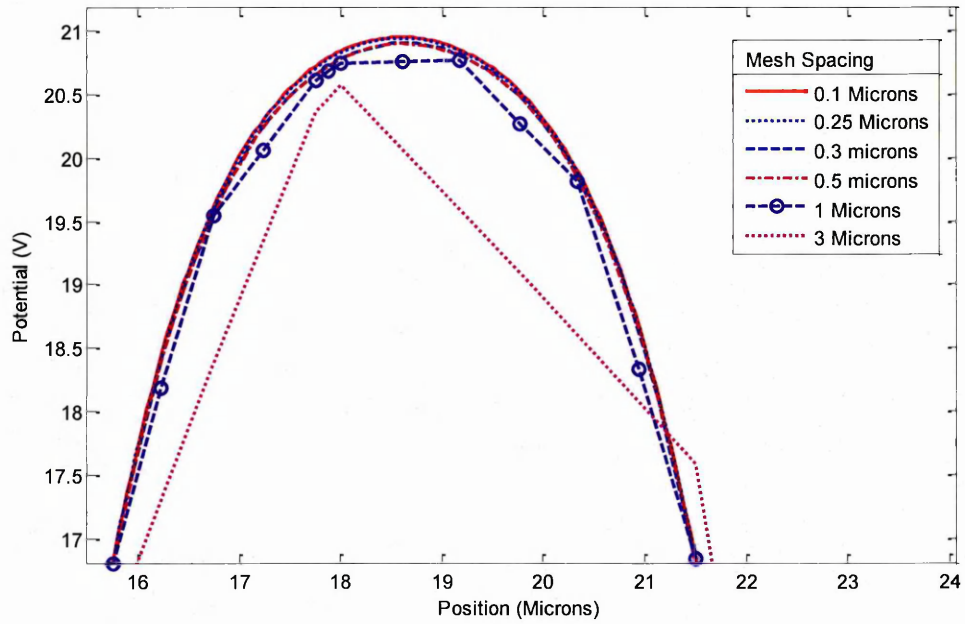


Figure 4.25: The variation in simulation output calculated for different mesh densities in the x-axis. Each model solves for the same device parameter (i.e. potential field) using a different mesh. The meshes are the same as those used to produce Figure 4.24.

In normal simulations the mesh can be altered in each dimension although only a single dimension was used in this example to simplify the description. Generally the density of the mesh layout in one dimension must be balanced against the mesh in the other dimensions of the model. A general rule for an initial mesh layout would be to use mesh spacing comparable to the smallest feature size in the immediate mesh area. In the x-dimension explored here, that would be the inter-electrode oxide gap of $\sim 0.25 \mu\text{m}$. Meshes much finer than this would result in an exponential simulation time increase for a minimal accuracy gain, as can be seen in Figure 4.25 and Figure 4.26.

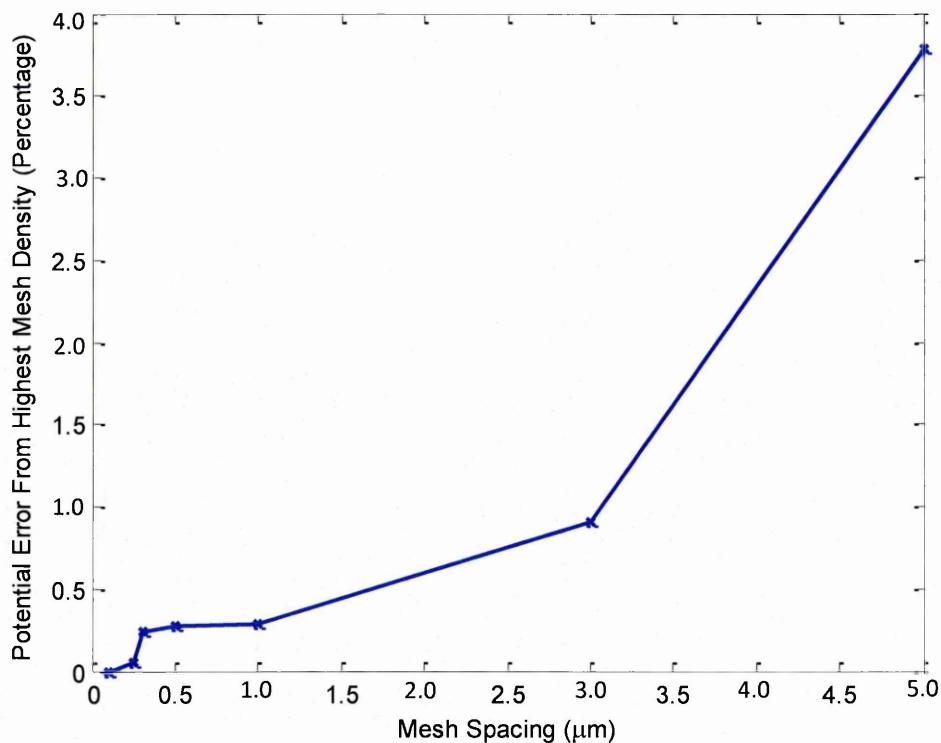


Figure 4.26: The percentage difference between the peak potential value, seen in Figure 4.25, across the different mesh densities when compared to the most dense mesh.

Figure 4.26 plots the difference between the peak potential values measured from Figure 4.25 across the range of mesh layouts, when compared against the value calculated for the most dense mesh. The potential is measured at the x-coordinate 18.5 μm from Figure 4.25. The potential values used for Figure 4.26 are linearly interpolated between mesh points for those models which contain fewer mesh points (where a mesh point may not lie at 18.5 μm).

4.1.2 Euclid CCD Model Geometry

This section details the development of device models for the Euclid CCD273 and CCD204 pixel and register structures. The CCD273 shares its pixel design with the CCD204. The devices differ in the layout of the readout register that is modelled for each device. The register in the CCD273 is redesigned from the CCD204 to offer improvements to serial CTI during radiation by reducing the serial register channel width. The redesign is based on the assumption that a smaller channel will reduce the charge packet dimensions and hence the number of traps encountered by it during charge transfer. The device geometries are obtained from CAD schematics produced during

design stages of manufacture (Personal Communication). The use of these schematics allows simulations to be produced that match the design dimensions exactly, but these take no account of manufacturing variation, which is discussed later in this chapter.

4.1.3 CCD273 Pixel Model

Gate geometries are an important parameter because they define the extent of the potential wells in the lateral dimensions, and are therefore directly related to charge storage mechanisms within the device. Device architecture will therefore have an impact on the results obtained from the models when charge packet data is explored.

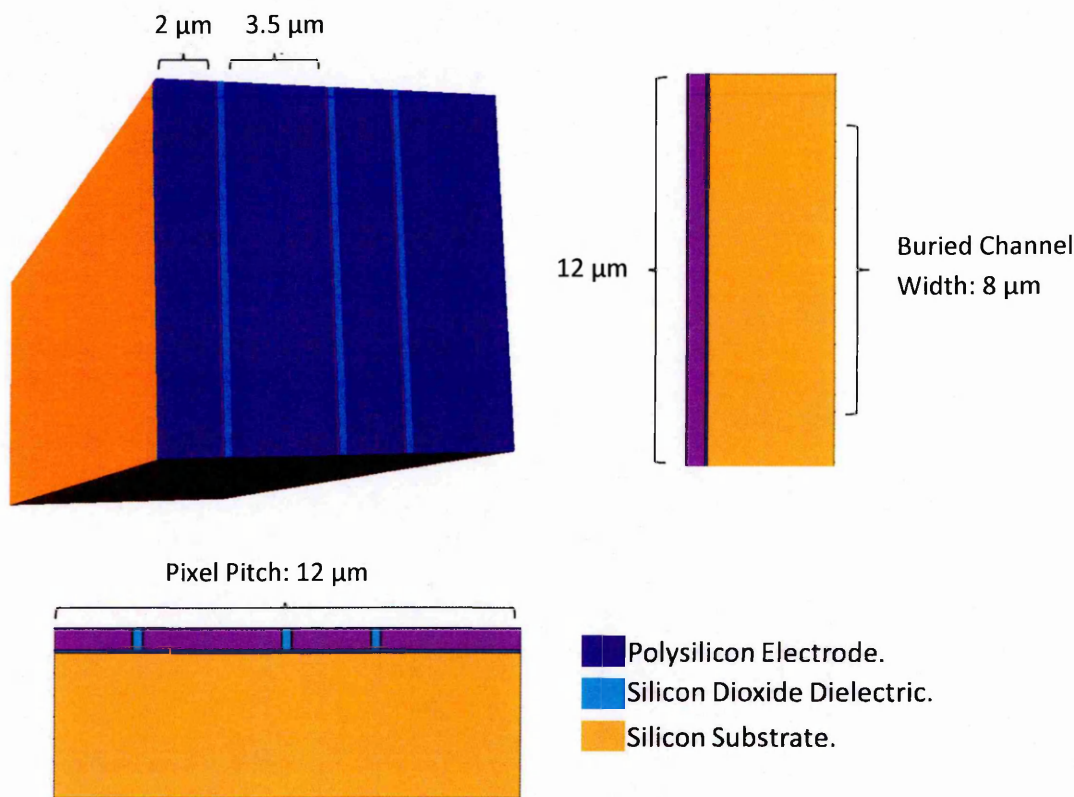


Figure 4.27: The 3D single cell Euclid pixel model alongside 2D cross sections which show the device structure in the along and across channel dimensions. The dimensions used to define the model are shown.

Both the CCD273 and the CCD204 share the same four-phase $12\ \mu\text{m}$ pixel design. The pixel electrode structure has an asynchronous gate layout with alternating $2\ \mu\text{m}$ and $4\ \mu\text{m}$ gates. Some allowance must be made for inter-electrode dielectric, and after consultation with David Burt, the e2v Chief Engineer, the larger $4\ \mu\text{m}$ gate is undersized at $3.5\ \mu\text{m}$. A typical $0.25\ \mu\text{m}$ inter-electrode

gap can now be used in the models, while keeping the total pixel size within the specified 12 μm pixel pitch (Figure 4.27).

The Euclid CCDs are back illuminated, and are designed on e2v's deep depletion process with a substrate thickness of 40 μm , back-thinned from a thicker substrate. This allows the depletion region to extend to within a few microns of the back-surface which improves charge collection at shorter wavelengths, where the majority of charge generation will occur close to the back surface where light is incident.

4.1.4 Register Model

The readout registers in the CCD204 and CCD273 follow the same basic design criteria (Figure 4.28). However, the CDC273 has a reduced channel width compared to the CCD204 in an attempt to improve the serial charge transfer efficiency (CTE). The channel width designed for the CCD204 is 50 μm , while the CCD273 has a much narrower 20 μm serial register channel.

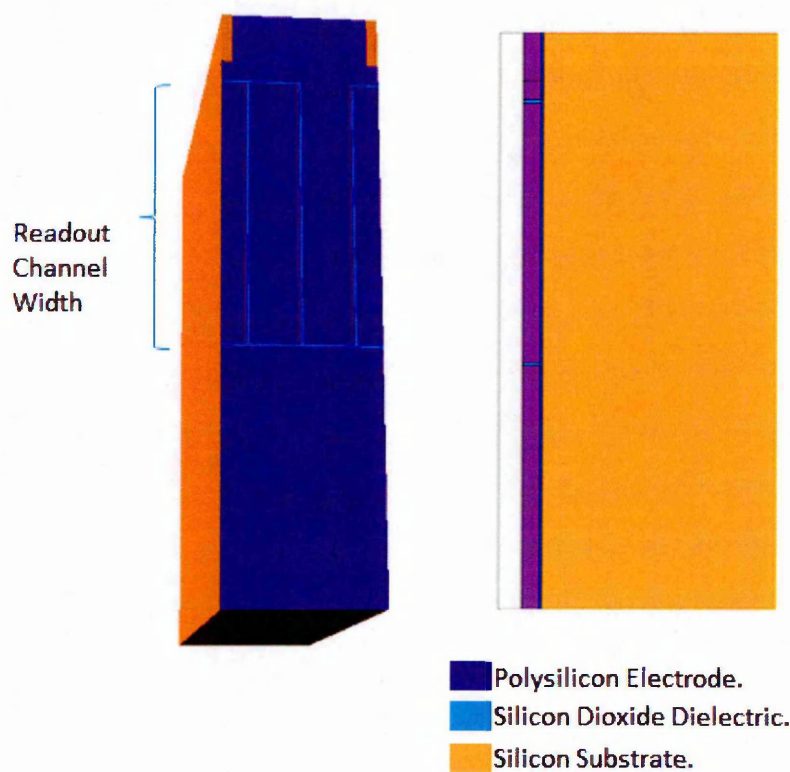


Figure 4.28: The 3D single cell register model alongside a 2D cross-section to show the gate structure. This same structure is shared between the CCD204 and CCD273, but with different channel widths (20 μm for the CCD273 and 50 μm for the CCD204).

The redesigned channel width was implemented based on assumed charge trapping behaviour, which effects CTI. As trapping is dependent on a charge packet coming into contact with a trap, by restricting the charge packets to a smaller volume the number of traps encountered will reduce proportionately, although the traps may be at a higher density at any trap sites. These assumptions are based on experimental evidence which has shown that smaller feature sizes result in a reduced effect from radiation damage in CCDs (Gow, et al., 2012).

4.1.5 Doping Specification

The CCDs currently base-lined for Euclid, as with all modern scientific CCDs, are “buried channel” devices. A layer of n-type silicon is created by doping the substrate with a layer of phosphorus at the surface. This forms a pn-junction a small distance into the substrate.

The depletion region, and hence the potential well, which form around the pn-junction are determined by the device doping. The doping profile used in the Euclid models was produced by e2v using a Silvaco Athena module SSuprem3 (Seabroke, et al., 2009), a one-dimensional process simulator. SSuprem3 outputs a simulated doping profile of net doping density (donor ions per cm^3) as a function of substrate depth (μm) based on a simulated doping process (Figure 4.29).

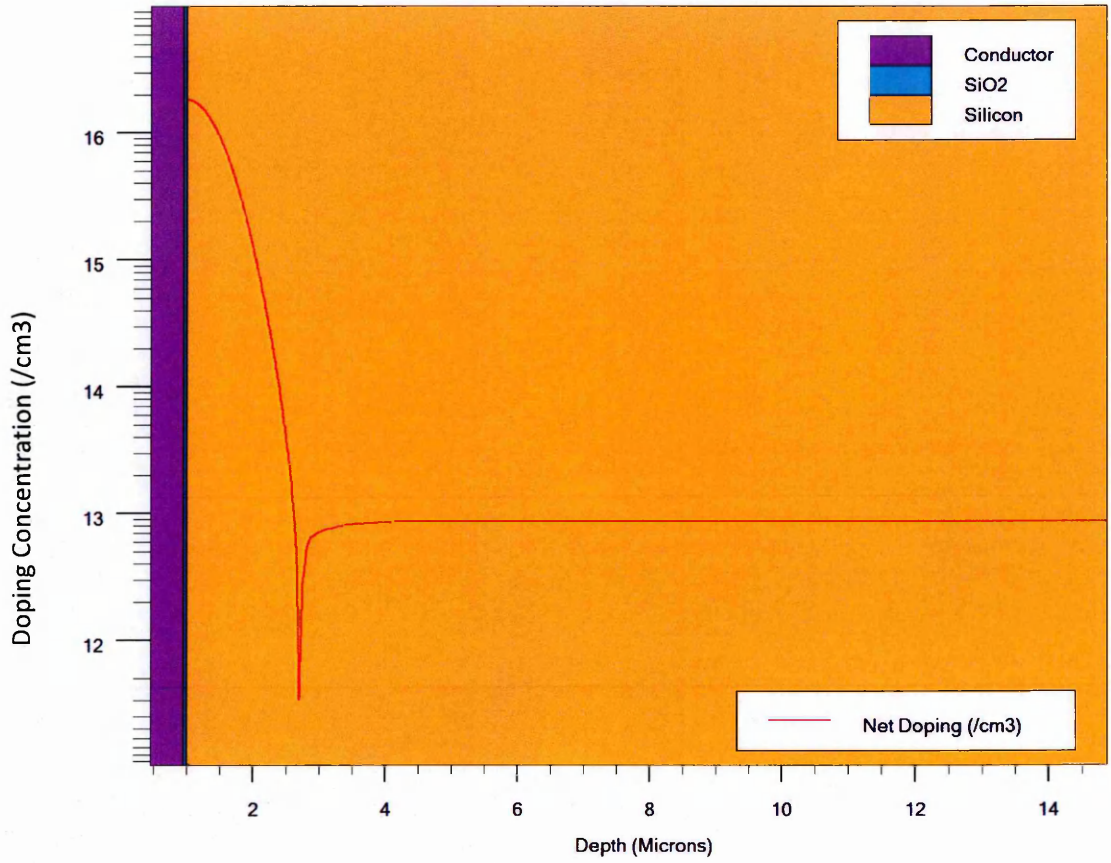


Figure 4.29: The Gaussian doping profile used in the device models produced using a 2D array of doping concentrations recorded against depth.

4.1.6 Dielectric Layer

The insulating oxide layer present in the Euclid devices consists of a layer of silicon nitride (Si_3N_4) and a layer of silicon dioxide (SiO_2). This composite structure is necessary for manufacture. To keep mesh complexity to a minimum, this region can be modelled as a single equivalent thickness of SiO_2 given by Equation 4.8. Where ϵ is the dielectric constant of each material and t is the thickness of each material layer (Seabroke, et al., 2010).

T_{eff} is the effective thickness of silicon dioxide which the composite layer represents, while T_{ox} and T_{nit} are the actual layer thicknesses of the silicon dioxide and silicon nitride respectively.

$$T_{\text{eff}} = T_{\text{ox}} + \left(\frac{\epsilon_{\text{ox}}}{\epsilon_{\text{nit}}} \right) \cdot T_{\text{nit}} \quad 4.8$$

4.1.7 Electrode Definition

The overlapping electrode structure normally seen in CCD schematics is omitted in these CCD models to reduce the complexity of the model mesh and keep simulation time to a minimum. A simple model can be used to evaluate the effect this has on the model parameters.

A 2D model of the Euclid device with the same geometry and doping as a 3D simulation is used because this allows more memory for allocating mesh points in the electrode structure and the extension of the model beyond a one-pixel cell in the along-channel dimension. The effect of gate overlaps is compared across several models with the same dimensions and mesh but different gate structures. The model has 12 gates in total; as this is a four-phase device there are three pixels, with the overlapping structure present on only one gate in the centre pixel to allow comparison of the potential wells.

Device structures simulated in the Silvaco ATLAS module must be made up of simple geometric shapes; this is why in the image presented in Figure 4.30 the overlapping structure of gate 6 appears to be made up of four separate conductors. In the model specification, although these are initially coded as separate conductors there is no gap between them and they are explicitly coupled to gate 6 and share the same work function, therefore they are treated as one gate by the simulation.

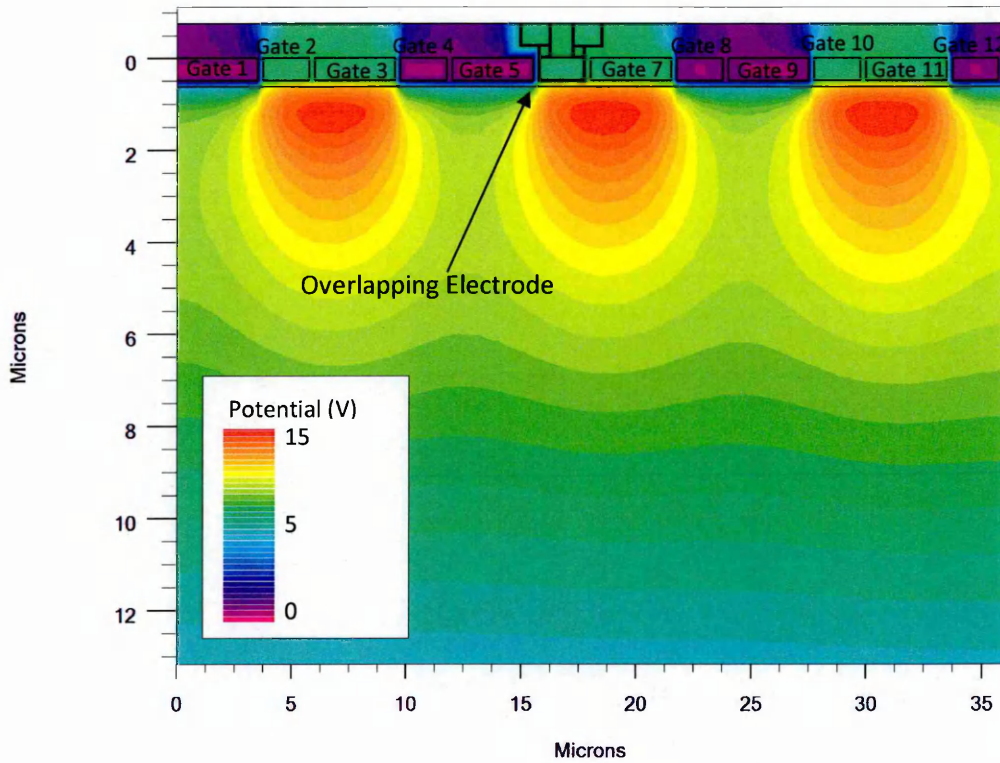


Figure 4.30: A 2D simulation to explore the possible effects of omitting gate overlaps from the device models. Only the centre pixel has overlaps included on one of the active gates which allows a direct comparison to the adjacent pixels.

The potential field contour plot (Figure 4.30) indicates that gate 5, the unbiased barrier phase adjacent to the overlapping gate structure, shields the substrate from the potential field generated by the overlapping section of gate 6. The same is true for the opposite overlap, except that gate 7 is biased to the same potential as the overlapping gate, so there is no net effect on the underlying field.

Overlaying the potential well from the centre pixel from two models, one with and one without overlaps, enables a direct comparison (Figure 4.31). There is no difference between the potential wells defined across the models with and without overlaps. Therefore modelling the Euclid pixel without gate overlaps to simplify the mesh will have no effect on the charge packet simulations.

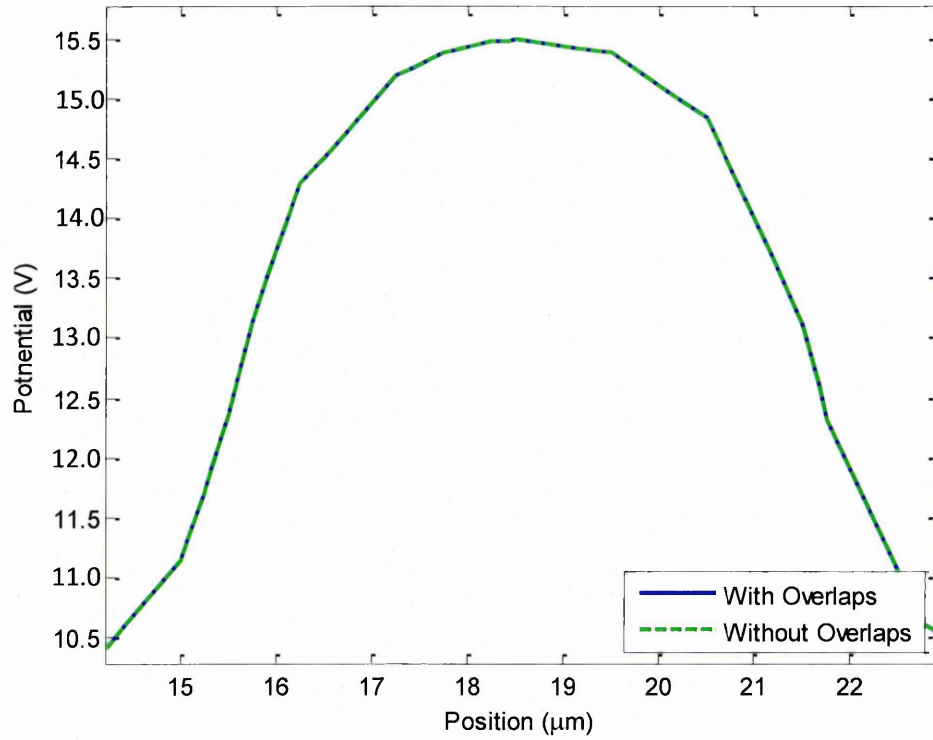


Figure 4.31: Potential well extracted from the centre pixel of Figure 4.7 and overlaid against the same model with no overlaps in the electrode structure. There is no difference between the potential wells, as such one of the colours (defining the potential well with overlaps) cannot be seen as it sits in the exact position as the other plot.

A slight distortion to the potential field appears across the model as a whole and is the result of mismatching electrodes at either end of the model (Figure 4.30). The model is terminated on the right hand side by the smaller 2 μm electrode, whereas the terminating gate on the left is the larger 4 μm , allowing a larger space between the model edge and the active pixel area. This causes a small but noticeable difference in the fields of the two outer pixels as the model boundary is approached, but this has a negligible effect on the centre pixel potential distribution.

4.2 Interpreting Model Data

It is possible to create both two- and three-dimensional models using Silvaco and extract data from these in one-, two- and three-dimensions. Contour plots in 2D are often used as an initial guide to check models are operating as expected, with field lines and quantities represented in varying colour levels. An example has already been seen in Figure 4.30. One dimensional data can be taken from the 2D contour plots and is primarily used for more accurate measurements of specific parameters, seen in Figure 4.25, Figure 4.29 and Figure 4.31.

CCDs are designed to complete two primary tasks: the collection of photo-generated charge and charge transfer. Both these tasks are dependent upon the electric and potential field structure within the device and charge collection is limited by the Full-Well Capacity (FWC). FWC is the maximum amount of charge that a single pixel element can contain before the potential wells of adjacent pixels become more attractive to signal charge causing charge to spill into neighbouring pixels. Driving the device beyond the full well capacity will result in charge spilling across barrier electrodes into adjacent potential wells, which causes blooming in captured images. Under some operating conditions the charge might preferentially spill towards the Si-SiO₂ surface interface where charge trapping due to the dangling bonds in the mismatched lattice will reduce CTE. Any spilling of charge is considered to be an indication of FWC being surpassed. FWC is determined through a combination of the buried channel doping, the device geometry and the voltage applied to the device electrodes.

4.2.1 Potential Field

The channel parameter (Φ_{ch0}) and FWC are two closely related device parameters that are also directly linked to charge storage characteristics. To understand the definition of these parameters in the device models it is necessary to understand the formation and characteristics of the potential well, which can be shown in data obtained from the Euclid pixel model.

In an n-channel CCD, such as the CCD273 used for Euclid, a depletion region forms due to the recombination of mobile carriers located around the junction between the n-type buried channel and the bulk p-type substrate region. Due to the lack of majority carriers in these regions a net

positive charge forms on the n-type side of the junction and a net negative charge forms on the p-type side. The regions on either side of the junction, which have become depleted of majority carriers, are known collectively as the depletion region. This region is characterised by a potential field similar to those seen in simple p-n-junctions. The potential increases from its minimum in the p-type substrate to its maximum within the n-type buried channel before falling off as the dielectric layer interface is approached to match the applied gate bias (Figure 4.32).

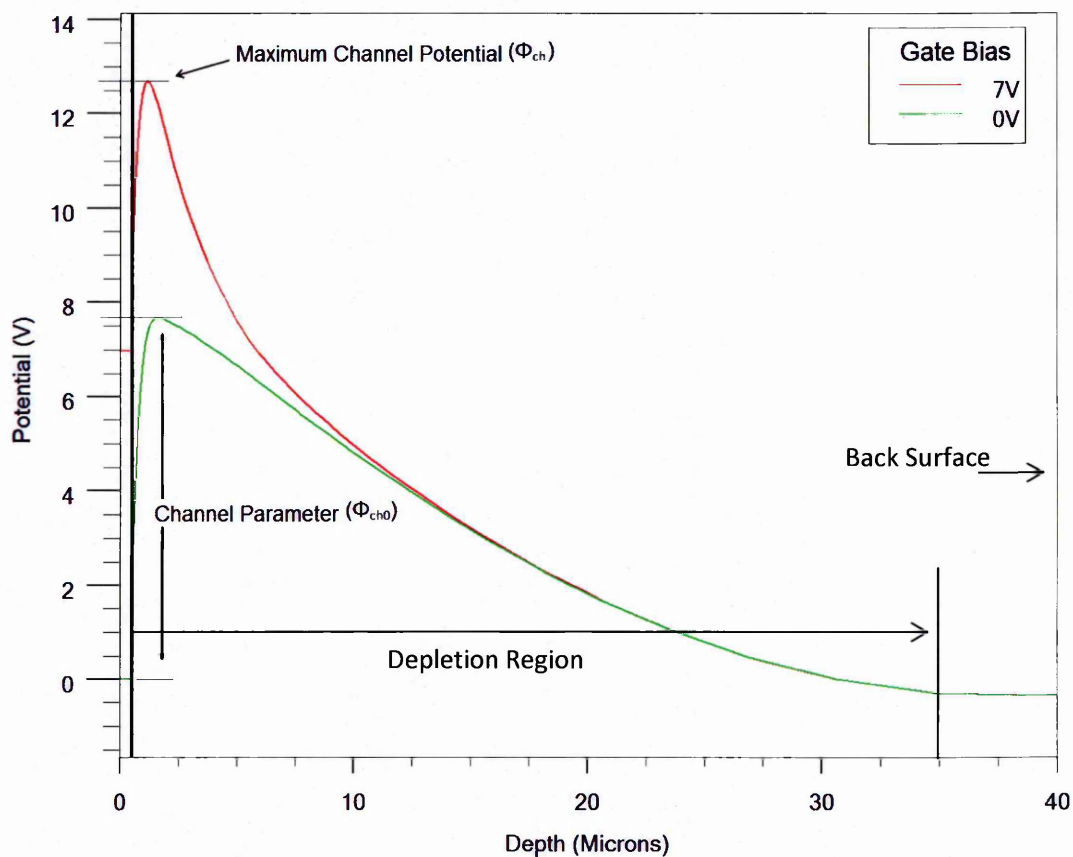


Figure 4.32: Potential field vs. depth into the substrate, showing the peak channel potential that defines the buried channel. The potential profiles for both biased and unbiased electrodes are plotted, where the unbiased electrode will act as a barrier to the charge stored under the biased gate.

Applying a positive voltage to the active gate electrodes reverse biases this junction, which increases the potential maximum in the n-type buried channel, as seen in Figure 4.32. Charge is attracted to, and collected in, this high potential area or potential well under an active (positively biased) gate electrode. Charge is held away from the surface interface because the voltage

applied to the electrode is negative with respect to the maximum channel potential (Φ_{ch}), owing to the high doping concentration associated with the buried channel.

The channel parameter (Φ_{ch0}) defines the potential difference between a zero voltage applied at the gate electrode and the potential that forms in the buried channel. The channel potential (Φ_{ch}) will always be higher than the applied gate voltage by an amount equivalent to $\sim\Phi_{ch0}$ when the device is fully depleted, Figure 4.32.

The potential maximum is slightly offset from the pn-junction location due to the difference in doping concentration and hence the change in fixed charge experienced across the junction. The buried channel actually lies within the n-type silicon, as the gate electrode bias increases the potential maximum and moves it closer to the surface interface.

A higher bias applied to a gate generally results in a larger FWC due to a larger potential well. However, as the potential well moves closer to the surface interface with increased bias, the probability of charge interacting with the surface increases. There is an operating voltage that enables the optimum FWC to be achieved, which balances Blooming Full Well (BFW) with Surface Full Well (SFW). Biasing higher than this optimum level will result in charge interacting with the surface at large signals. When the bias is lower than optimum, charge will spill into adjacent pixel wells. The latter is preferential because charge transfer efficiency will be preserved even at the highest signal levels.

4.2.2 The Effects of Charge Storage

During charge collection, signal charge which is photo-generated within the depletion region of the CCD substrate is attracted to the local potential maximum (Φ_{ch}) which is commonly referred to as the potential well. During charge collection a section of the depletion region within the potential well becomes un-depleted, as the charge carriers collected compensate the fixed ions in this area. The build-up of charge results in a reduction of Φ_{ch} proportional to the number of charge carriers present in the signal packet (Figure 4.33).

Full Well Capacity (FWC) may theoretically be achieved when the peak channel potential has reduced, due to charge collection, to a level which is comparable to the maximum channel potential of an adjacent “off” (barrier) electrode. Collecting charge in the potential well beyond this limit will result in the electrons having enough thermal energy to surpass the “potential barrier” represented by the barrier phase, and begin to “spill” along the channel into the potential wells of adjacent pixels, a process known as blooming.

The potential maximum moves towards the surface as charge accumulates in the potential well, (Figure 4.33) increasing the probability of charge also interacting with “dangling bonds” at the Si-SiO₂ interface. When this interaction occurs a fundamental limit to the well capacity has been surpassed, because interaction with these bonds will significantly reduce CTE. This condition is known as Surface Full Well, where this occurs before blooming it is a consequence of higher than optimum gate biasing (Janesick, 2007).

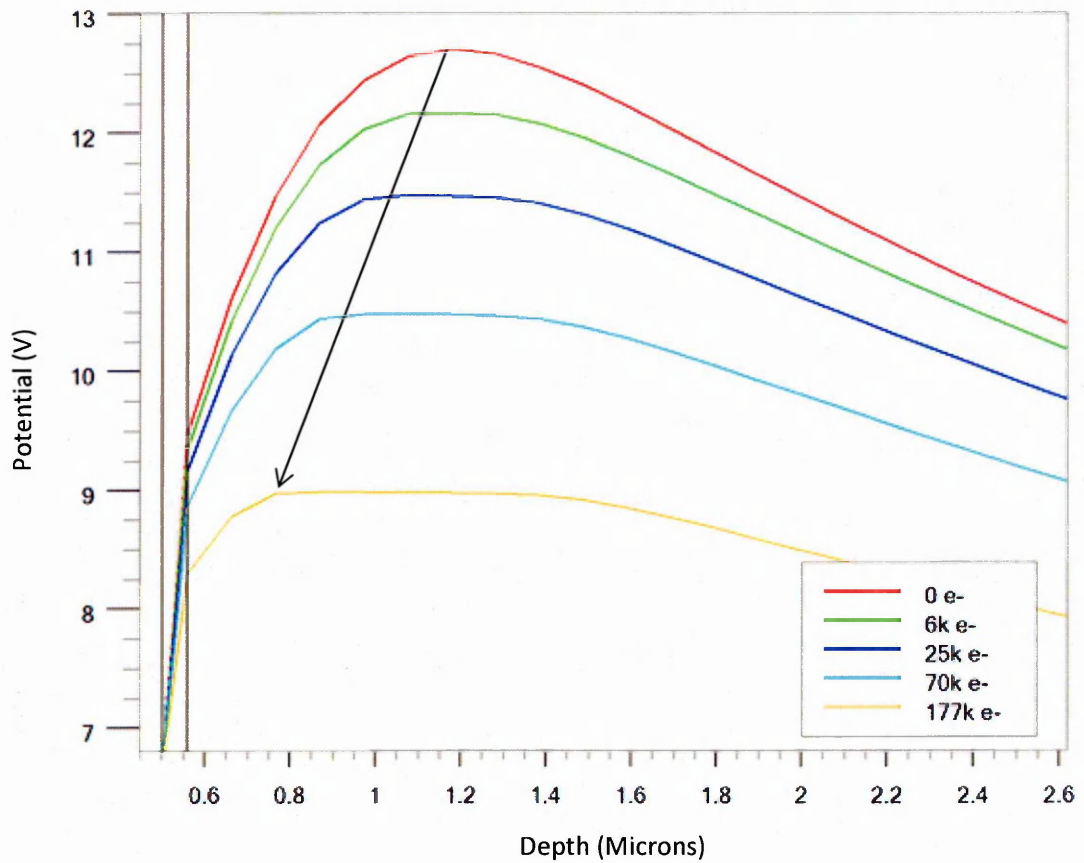


Figure 4.33: The effect of charge accumulation on the potential field structure. The potential maximum reduces in proportion to the number of charge carriers present and the peak of the potential well moves closer to the surface interface.

As charge concentration in the potential well increases, the potential difference between the surface interface and the channel reduces, increasing the probability of a charge carrier surpassing this potential. The mutual repulsion due the electric field produced between two electrons will act to encourage charge out of the well. Similarly, thermal energy from the lattice can be passed to the electrons giving them enough energy to surpass the potential barrier, an effect known as thermionic emission (Janesick, 2007). If electrons can gain enough energy to surpass the potential barrier presented at the edges of the potential well, the Surface Full Well limit of the pixel has been reached.

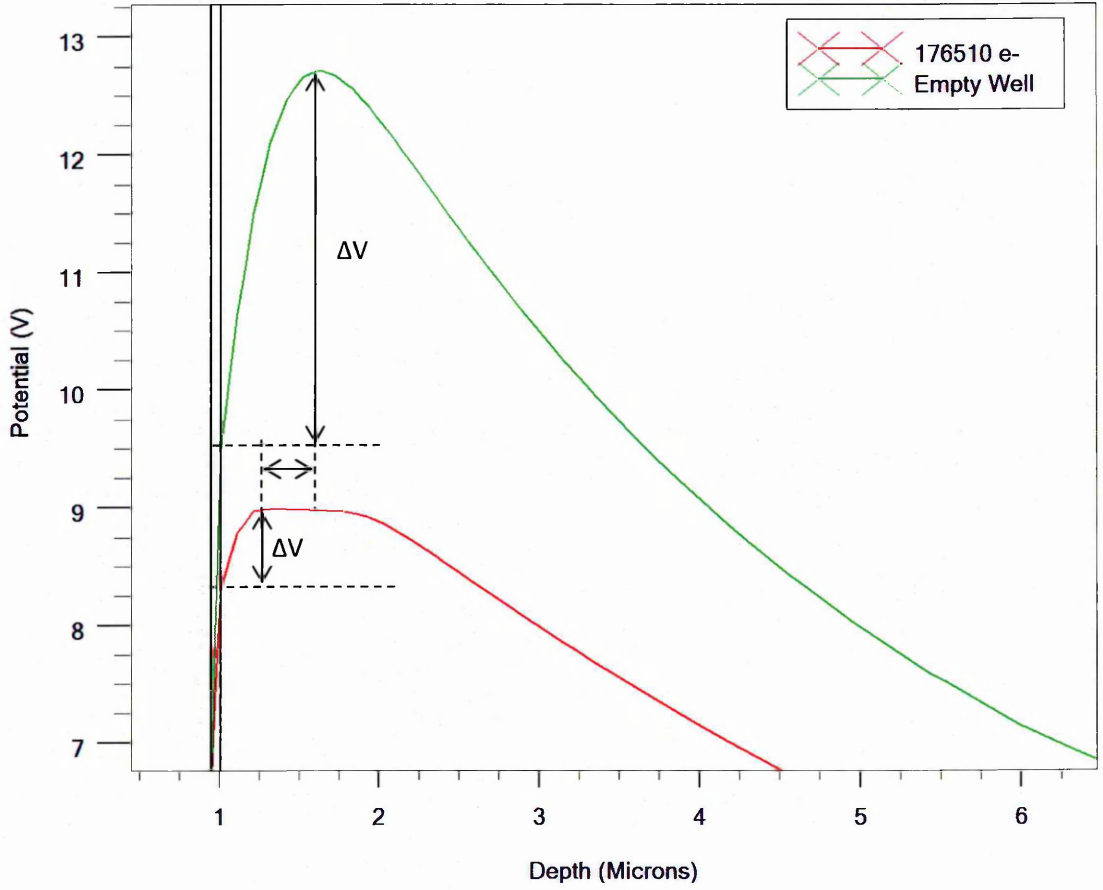


Figure 4.34: The Potential barrier, ΔV , presented to charge packet electrons at the surface interface. This changes as charge builds up in the potential well and determines the point at which charge might “spill” according to Equation 4.9.

The probability of an electron crossing the potential barrier can be described by Boltzmann statistics (Janesick, 2007), as shown in Equation 4.9 (where ΔV is the potential difference between the channel potential and surface potential, k is Boltzmann’s constant (J/K), T is the absolute temperature (K) and q is the charge of an electron (C). kT/q gives the average thermal energy of an electron in volts (the thermal voltage). Equation 4.9 is used to analyse the Silvaco device models to ensure that the SFW limit has not been surpassed when modelling Full Well Capacity (FWC), as described in the next section.

$$P = \exp\left(\frac{-\Delta V}{kT/q}\right) \quad 4.9$$

It is also possible to plot the potential field across the pixel in the direction of charge transfer. The potential profiles in Figure 4.35 are similar to those in Figure 4.33, except these are plotted across the lateral pixel dimension at a depth of $\sim 1 \mu\text{m}$. The values extracted from these plots will vary depending on the measurement depth. Therefore the potential difference between the channel potential under the active and barrier phases, which defines the pixel well, will vary depending on the measurement depth. The lateral potential field is plotted in Figure 4.35; the barrier phases on either side of the pixel differ due to the asymmetric gate geometry defined in the Euclid pixel.

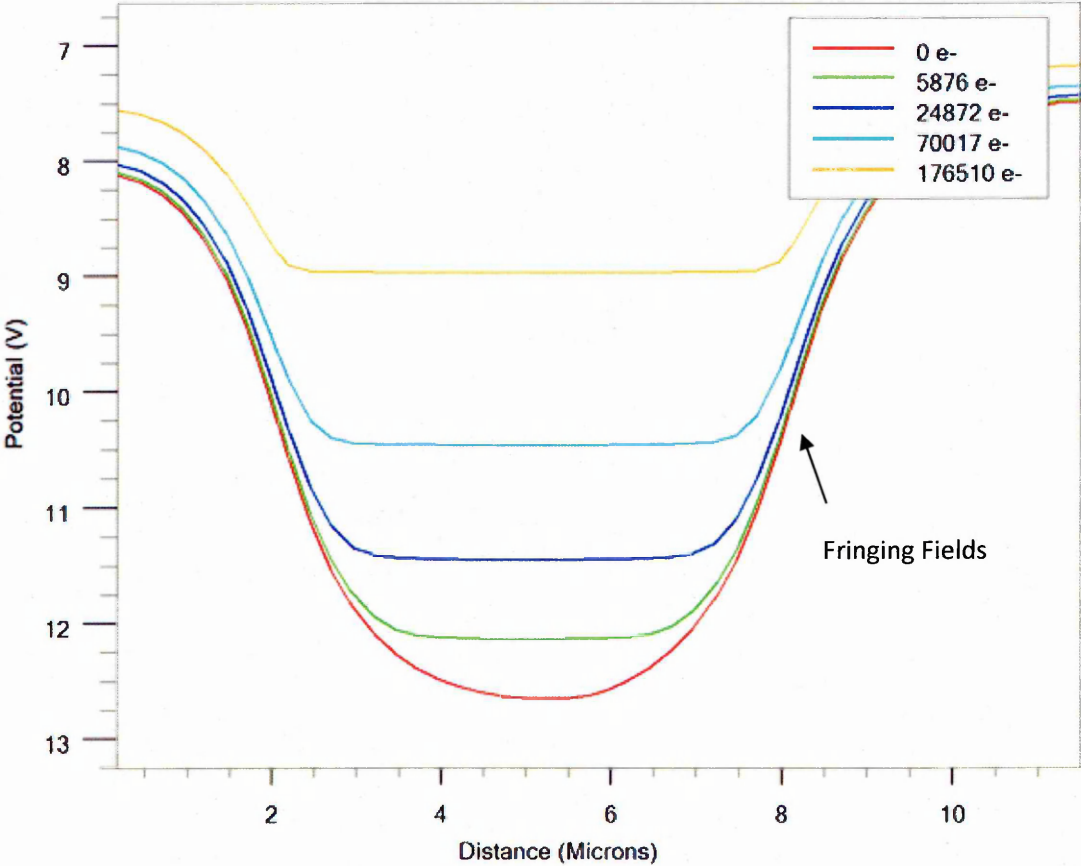


Figure 4.35: The effect of charge accumulation on the potential well structure. The potential maximum reduces as signal charge increases reducing the barrier potential to neighbouring structures.

4.2.3 Modelling Full Well Capacity in 2D

An initial 2D model was developed for exploring the effects of charge collection and developing a method for defining the FWC in the CCD models. A 2D model enables the simulation of multiple pixels while using a complex mesh in a single plane. Charge carriers are introduced to the storage well in the centre pixel until they begin the spill laterally into the adjacent pixels, indicating a full well condition. Two-dimensional simulations have a fast runtime, so are often used to test measurement techniques quickly before being applied to more complex 3D models. The three-pixel model would be impractical in 3D due to the size of the model mesh, the run-times involved (~several days) and the amount of memory needed for the simulation.

There are a number of ways in which charge carriers can be introduced into a simulation. In this model a 1 μm wide collimated beam of light is simulated; it is incident at the centre of the back surface of the model. The simulated light source has a wavelength of 400 nm in the blue light range, which is within the expected visible range typically expected for the Euclid detector. It will have a higher probability of absorption near the back surface where it is incident, with an estimated absorption depth of $\sim 0.2 \mu\text{m}$ (Janesick, 2007).

The model solution presents the charge packet as an electron concentration per unit volume ($\text{e}^- \cdot \text{cm}^{-3}$) versus the position within the device. This can be displayed in a contour plot, such as that in Figure 4.36, which shows the charge concentration in the device model while the beam is active. Charge is generated around the beam location signified by a higher charge concentration, it is then swept towards the potential wells under the active gates, while some migrates laterally to the outer pixels. The majority of the charge generated is collected in the active area in the centre pixel where the beam is incident.

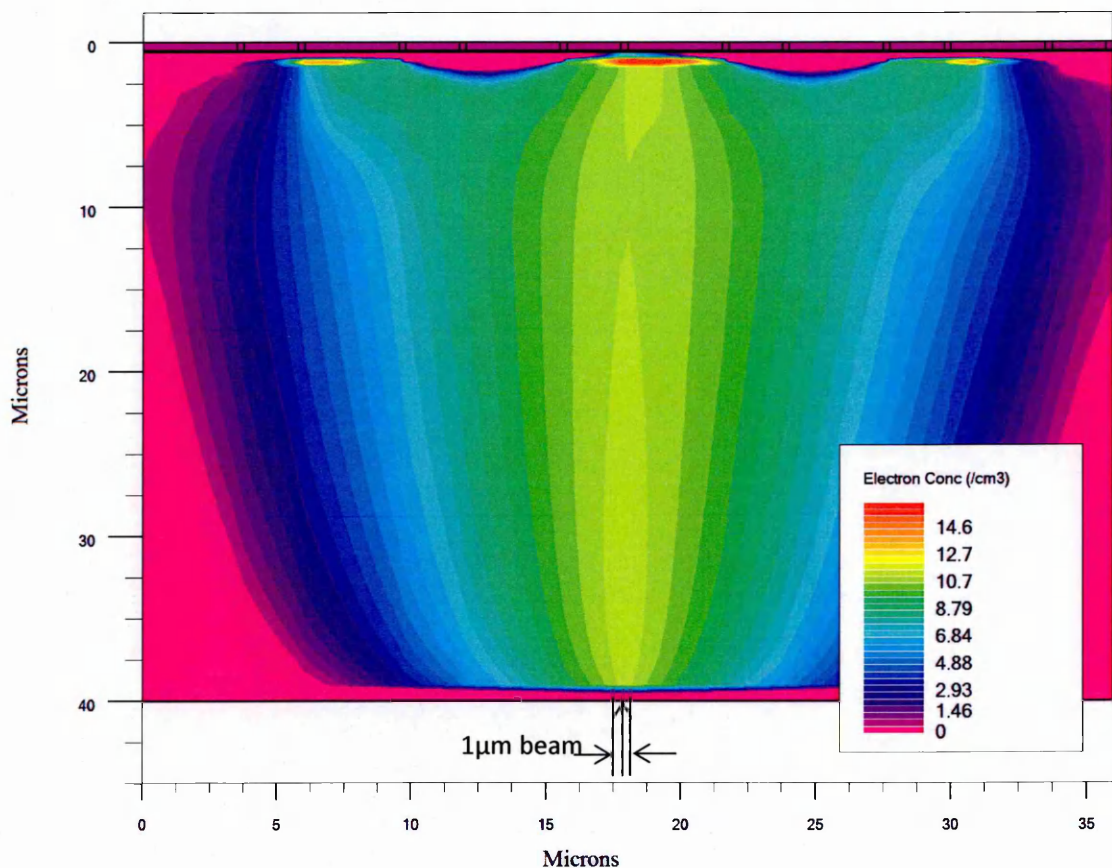


Figure 4.36: Electron concentration contour plot generated when a 1 μm collimated beam is incident on the back face of the CCD at x location 18 μm , the electron concentration contours are logarithmically scaled, so should be taken as $10^x/\text{cm}^3$, where x is the electron concentration indicated by the plot key.

The electron concentrations displayed on the contour plot of Figure 4.36 are presented in a logarithmic scale, (i.e. the colours range from 10^1 to 10^{15} e-/ cm^3). Therefore some of the areas that appear to have charge present, the blue and some of the green areas, are actually very small concentrations and may be regarded as negligible.

The beam is on for a defined time period before it is deactivated and the generated charge is allowed to collect in the potential wells under active gates. The amount of charge collected in an individual pixel can then be measured by integrating the electron concentration over the pixel area. The total charge in all three pixels will always be 100% of the electrons generated in this model. By measuring the charge in each pixel individually as the intensity of the beam in the simulation is varied gives an opportunity to plot the charge accumulation in the pixels versus the

total amount of charge present, for a given intensity. In this model the centre pixel should accumulate more charge than the outer pixels, because the beam is directed at it. Figure 4.37 shows a plot of charge accumulation in the model, focussing on the centre pixel.

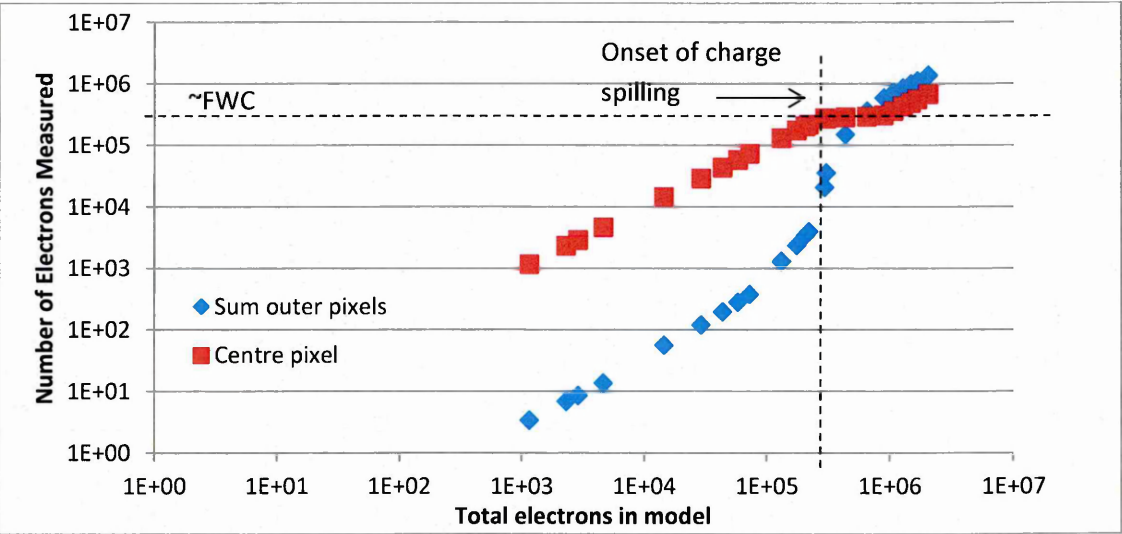


Figure 4.37: A model of charge accumulation in adjacent pixels based on the 3 pixel model with optical beam incident on the centre pixel, shown in Figure 4.13. The number of electrons collected in each pixel is measured and plotted against the total number of electrons in the model. The amount of charge in both the centre and the outer pixels increases linearly until the centre pixel becomes saturated, when more charge is collected in the outer pixels.

The intensity of the incident beam is varied while keeping the integration time (the time that the beam is on and the CCD model active) constant, this generates a series of models with varying signal sizes. The signal collected in each pixel is then measured as previously outlined and the results are plotted. Figure 4.37 shows a plot of the amount of charge collected in the centre pixel against the total charge present in the model, and the sum of the charge in the outer pixels against total charge in the model. Summing the charge present in each pixel gives the total charge present in the model.

The plateau in charge collected by the centre pixel coincides with a large increase in the charge collected in the adjacent (outer) pixels, indicating the characteristic charge spill of the FWC limit. At the onset of the charge spilling in Figure 4.37, the signal in the centre pixel is measured at $\sim 2 \times 10^5 e^-$.

The information presented in Figure 4.37 indicates the signal level when FWC has been achieved. Figure 4.38 shows the same information which has been processed to give the charge in each pixel as a percentage of the total charge in the model. This gives a clearer indication of where the accumulation of charge in a given pixel is no longer linear due to charge spilling from the center to the outer pixels.

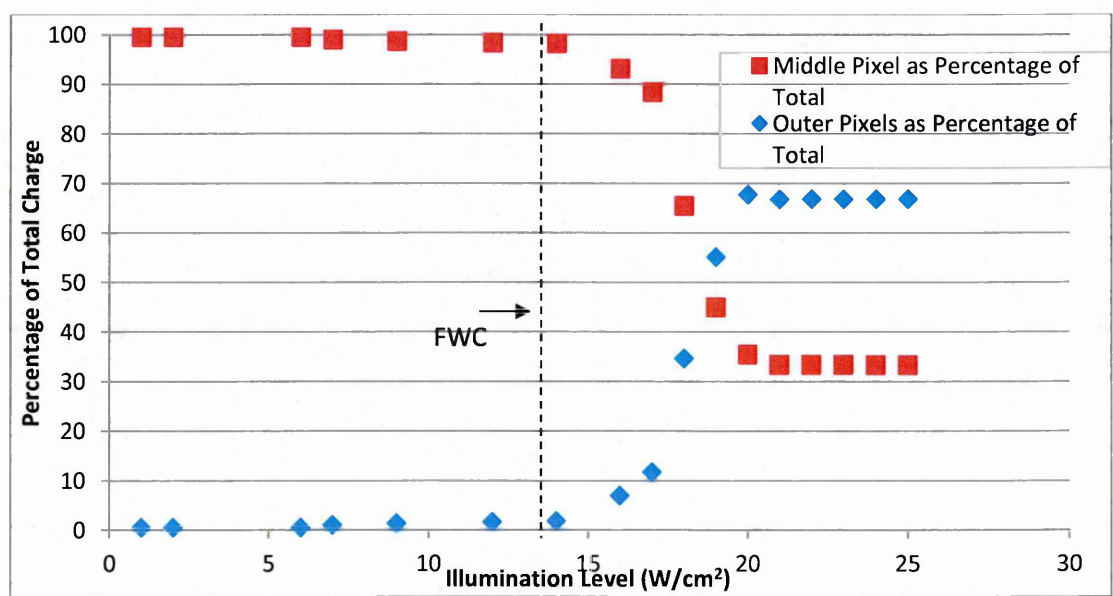


Figure 4.38: The amount of charge in each of the centre and outer pixels of the model shown in Figure 4.36, as a percentage of the total amount of charge. This gives a clearer indication of the FWC value during measurement.

A 2D contour plot of the charge concentration in one of the models at the onset of blooming is shown in Figure 4.39. The potential difference between the peak of the potential well and the barrier phase determines the blooming condition, proves it is possible for the charge collected to surmount the barrier and travel into adjacent potential wells. This barrier potential will vary within the same model depending on the measurement position. A simple plot of potential in the lateral dimension at varying depths at the full well condition gives the variation in potential barrier with measurement position (Figure 4.39). The potential well structure across the model also shows the difference in potential field at the edges of the model due to the mismatching boundary electrodes. However, this mismatch will have a negligible effect on the potential well of the centre pixel, and hence the calculated FWC.

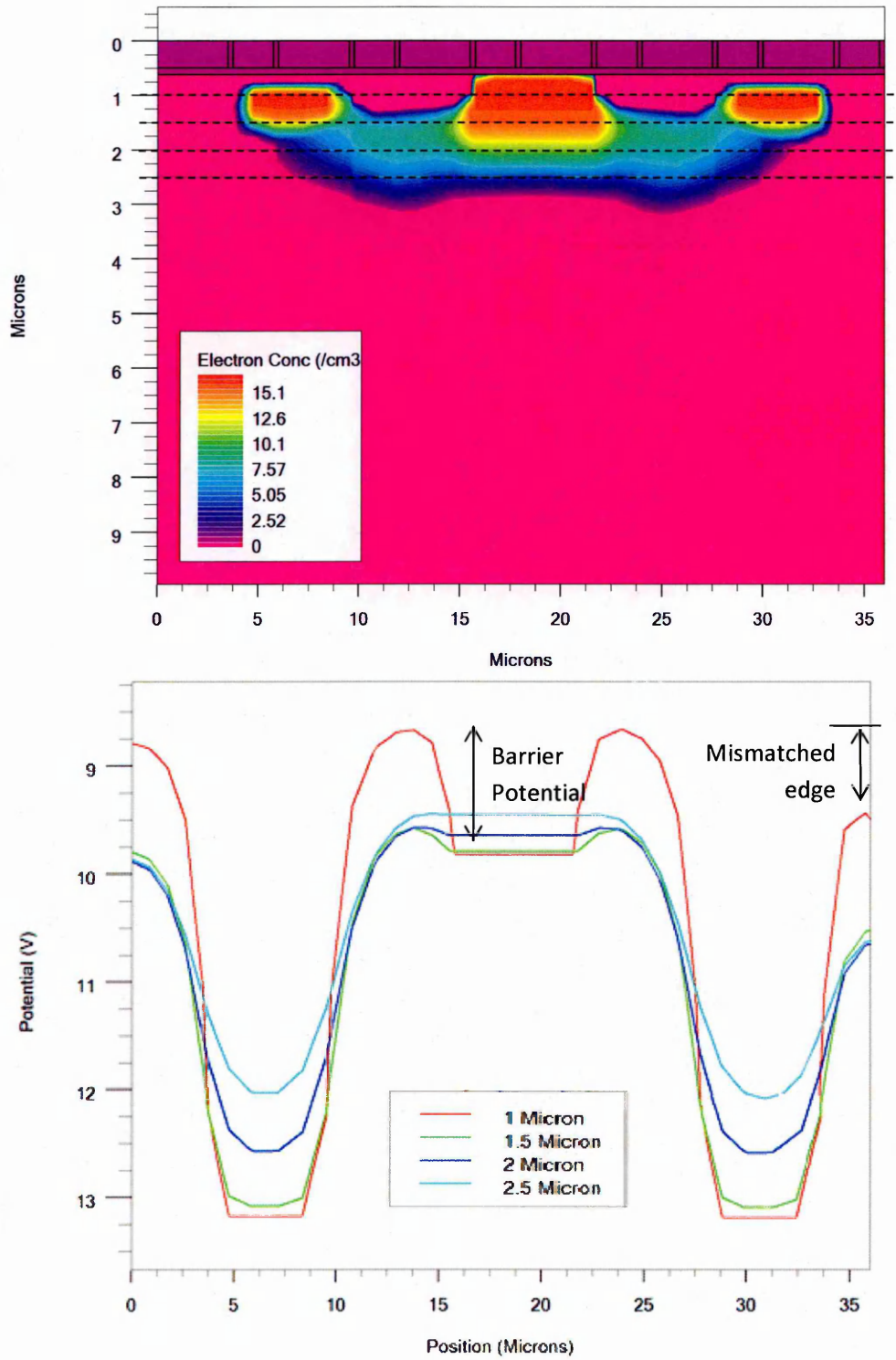


Figure 4.39: Electron concentration and the potential well structure at FWC, plots taken at increasing depth into the substrate from 1 - 2.5 μm (dotted lines on upper figure) to measure the effect on the barrier potential (ΔV) at different measurement points (presented in lower figure).

Figure 4.40 shows the barrier height presented by the potential wells between the centre and one of the outer pixels, where its variation depends on the measurement position as indicated in Figure 4.39. Figure 4.39 indicates that the path that the blooming charge takes between pixels is located at a substrate depth of between $1.5\mu\text{m} - 1.7\mu\text{m}$, measuring the potential barrier here gives a value of $\sim 0.15\text{ V}$ at blooming (Figure 4.40).

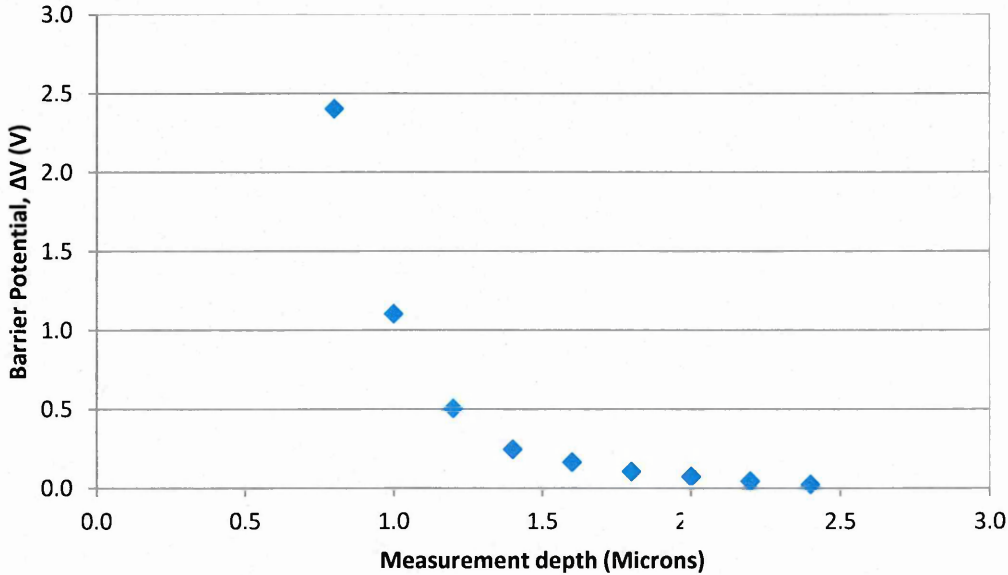


Figure 4.40: Barrier potential versus measurement position in terms of substrate depth extracted from the model presented in Figure 4.39. The potential varies depending on the measurement position, due to the doping density at each location and the signal size.

The transfer path taken by the blooming charge is determined by the minimum potential barrier needed to prevent blooming. The same doping profile is used across both 2D and 3D models, meaning the charge transfer path during blooming should be the same in both the 2D and 3D models.

4.2.4 Modelling Full Well Capacity in 3D

Three dimensional models can represent several orders of magnitude more computing complexity for simulation than the 2D models seen so far. Where the number of node points in a 2D mesh is multiplied by the number of planes representing the third dimension. Comparing the number of

node points in the model mesh between 2D and 3D models gives an idea of the difference in model complexity. The 2D model used in Figure 4.36 has ~4000 grid points in the two dimensional plane representing three pixels. By comparison a 3D model of a single pixel cell can consist of over 130,000 grid points, where there are up to ~1600 grid points per plane and as many as 80 planes making up the 12 μm device width.

It is possible to measure the FWC in 3D devices using the same method as in the 2D model in the previous section. The number of planes used to represent the extra dimension increased from one, in the 2D model. In this example the number of planes is increased to 22. The total mesh consists of just over 92,000 grid points, which is a significant increase on the initial 2D model, which had ~4000 mesh points.

A beam of the same wavelength (~400 nm) used previously is incident on the model in the same central position on the backside of the device. The FWC calculated from this 3D 3 pixel model is determined using a similar plot to that obtained from the 2D model of Figure 4.37. The FWC estimated should be more accurate due to the use of 22 planes representing the device width. The FWC calculated from this model comes out at $\sim 2 \times 10^5 \text{ e}^-$, which is very similar to the value calculated from the 2D model, which predicted a FWC of 2.1×10^5 electrons.

4.3 Conclusions

Device modelling using TCAD software packages requires only device architecture, doping and biasing to be accurately specified. Device parameters, which are well characterised in a laboratory environment, need an appropriate physical definition in the cell models to be measured. This is usually based on the analysis of the potential or electric field in relation to changing parameters such as electron concentration, but in some cases a direct analysis of the electron distribution is necessary when analysing charge packets – which are unique to CCD type devices.

Some consideration is made towards device solutions when specifying the model mesh where hardware memory, computational complexity and solution time need to be balanced. In many cases model complexity can be kept to a minimum by focussing on areas of interest and

simplifying periphery structures, which have a negligible effect on the parameters of interest, such as the poly-silicon electrodes.

Initially it was assumed that the potential barrier at the edges of the potential well might be used to analyse the FWC of a single cell pixel model through the use of Boltzmann's statistics (Equation 4.9). However the potential difference between the well and the barrier phase varies with the measurement position as shown in Figure 4.40, so is only suitable for determining surface interaction. It was decided that FWC may be calculated using a simplified 3D model with a reduced number of planes defining the device width. This would not be suitable for direct measurements of the charge packet, but is adequate for calculating a FWC estimate to compare against the value calculated in the 2D model.

4.4 Summary

The chapter was split into two main sections, model specifications and interpreting results which are extracted from them. The first half of the chapter introduced the main concepts surrounding semiconductor device modelling in TCAD, showing some of the concepts behind parameter calculations and giving guidance on model design techniques, with examples showing the effects of mesh specification. The second half of this chapter described techniques for extracting the data necessary for model verification which is presented in the latter half of this thesis.

Chapter 5: Charge Storage Characteristics

CCDs perform two main functions, the storage of charge carriers generated through the photoelectric effect and transferring the collected charge to the output node for measurement. Charge carriers, which are generated by photons incident on the device substrate, are swept towards the buried channel by the potential field that forms around the depletion region. The charge is confined in this electrostatic field until the device is read out, at which point it is transferred sequentially to the storage area under adjacent electrodes until it reaches the readout node.

This chapter focuses on the distribution of charge in the potential wells during the storage interval, which is modelled using Silvaco TCAD. Charge packets cannot be directly observed in lab based experiments because the CCD is a closed system, but the data presented here are important for understanding how device functionality may be affected by the charge storage characteristics and the optimisation of any future design iterations.

Charge transfer inefficiency, or CTI, has been a popular subject of CCD research for many years. With the development of the European Space Agency's Gaia mission to map star positions, CTI research took on a new significance. Due to the need for high accuracy in the Gaia mission, correction algorithms will be applied to the data to estimate CTI free images. Correction algorithms were first developed for the Hubble Space Telescope (Massey, 2010), but have been further refined through campaigns of charge trap characterisation and modelling for other space based telescopes (Massey, 2010) (Prod'homme, et al., 2011) (Rhodes, et al., 2010). The Gaia research was performed alongside a program of hardware improvements to mitigate the effects of radiation damage and shares many characteristics with the current development of the Euclid mission (Seabroke, et al., 2013).

The mechanism of electron trapping, as described in Chapter 2, causes an increase in CTI when the trap emission time is longer than the pixel dwell time. The later re-emission of charge captured from the signal packet causes the "charge tails" visible on captured images. These charge tails may alter the galaxy shape measurements performed as part of Euclid's weak lensing

survey. Alternatively a trap with a very long emission time may only re-emit captured charge after the entire image has been read-out of the device, in which case the signal level will be reduced (Hall, et al., 2012). In this way an image produced by a radiation damaged CCD can become distorted.

Electron trapping depends upon the trap interacting with the charge packet. Assuming that the proportion of the device buried channel occupied by the charge packet increases with the signal size, it is feasible that a trap close to the edge of a pixel will only trap at or near device full well capacity, whereas a trap in the centre will trap both at small and high signal levels. Thus CTI can vary depending on the signal level at which it is measured (Hall, et al., 2012).

Typical signal levels for the Euclid mission are expected to be in the range of 90 electrons background and 200-300 electrons for the objects of interest, where the Euclid device has an estimated FWC up to $\sim 1.9 \times 10^5 e^-$. At the typical signal levels trap interaction would heavily depend on how charge is distributed within the device at small signal, thus device modelling to predict charge distribution is essential for understanding trapping effects.

The effect of CTI on captured images is an important consideration for the Euclid device, where a charge tail caused by charge trapping can distort the PSF of a point source, such as a star, or the shape (ellipticity) of a distant galaxy. Considering that the weak lensing survey, which is an integral part of the Euclid mission, will be measuring similar small distortions in the shapes of astronomical objects, it is essential that these effects can be differentiated. With modern image processing techniques astronomers can correct for a large proportion of the CTI afflicted images to reconstruct CTI-free astronomical data (Massey, 2010). The models of charge packets presented here should go some way to increasing the understanding of device operation and improving some of these image processing techniques.

The Euclid CCD273 has a redesigned serial register as compared to its predecessor, the CCD204, which restricts the charge packet to a narrower channel. This was done with the aim to reduce the number of interacting traps and thus improve CTI by restricting the charge packet to a smaller

active area. These assumptions can be explored in the device models by comparing the relative change in the charge packet across the redesigned structures. Later chapters are focussed on finding a link between the theory presented here and real-world CTI measurements.

5.1 Charge Packet Modelling

Charge packets are an area of debate that is increasingly important for the high accuracy required in corrected images for astronomical surveys. Some existing work was introduced in Chapter 2, while this chapter presents the charge packet information that can be extracted from Silvaco.

The effect of radiation damage in CCDs is a major research topic that develops an understanding of the effects that the space radiation environment has on solid state detectors (Waczynski, et al., 2001) (Pickel, et al., 2003) (Hopkinson, et al., 1996). Charge packet modelling has been performed to try and describe the evolution of a charge packet depending on its signal size, which will aid the understanding of the charge trapping mechanisms observed in scientific CCDs. Radiation damage tends to distort images and reduce the signal to noise ratio through its effect on CTE, seen previously in Figure 2.7. These are serious problems which can affect the high accuracy requirements of Euclid's weak gravitational lensing survey. This survey requires a high level of knowledge of the detector PSF in order to obtain accurate image shape characteristics (Laureijs, et al., 2012).

CTI is a device parameter which is dependent on the signal size; as it is a measure of the percentage of charge left behind at each pixel transfer it tends to decrease as signal size increases (Waczynski, et al., 2001). CTI increases with radiation exposure as this will increase the concentrations of bulk traps, which are the main contributor to CTI (Hopkinson, et al., 1996). Charge packets will only be affected by a trap if the two come into contact. Thus as the signal size increases, the charge packet occupies a larger volume and will interact with traps which would otherwise be outside the charge packet distribution. If these assumptions are correct the volume which the charge occupies in the transfer channel is an important parameter to estimate an effective improvement in performance from the re-designed register geometry, such as those in Euclid CCD273 compared to its predecessor the CCD204. There are existing theories that describe

the charge packet volume, based around the analytical Charge Distortion model, or CDM (Short, et al., 2012) as described in Chapter 2.

5.2 Silvaco Charge Distribution

The models developed for this study have been introduced previously in Chapter 4. These consist of single pixel 3D models with a solution mesh optimised for measuring charge packet parameters. The solution for the electro-static potential field is calculated before the charge is generated as this determines the eventual location of the charge packet. The potential field is modified as electrons are introduced due to the compensating effect on the fixed ions in the depletion region around the buried channel, as discussed in Chapter 4. The Silvaco device models allow photo-generation to take place through a beam specification based on beam width, intensity and light wavelength, which each affect the numbers of electrons generated, along with some of the defined model parameters, such as the mesh density. In this study, the beam width and wavelength remain constant, while the intensity of the light is varied to change the signal level in the model.

The models are solved based on the expected operating conditions for the Euclid devices, where two integration phases are active for charge collection, leaving two inactive (off) electrodes to act as the charge barrier between pixels. Figure 5.41 is given as an example of the evolution of the charge packet in the along channel dimension for signal sizes ranging between 5000 and 172000 electrons. Electron concentration is highest in the centre of the active area, the concentration reduces exponentially as the edges of the active area are approached until the concentration becomes negligible which causes the “fuzzy edges” commonly described for charge packets.

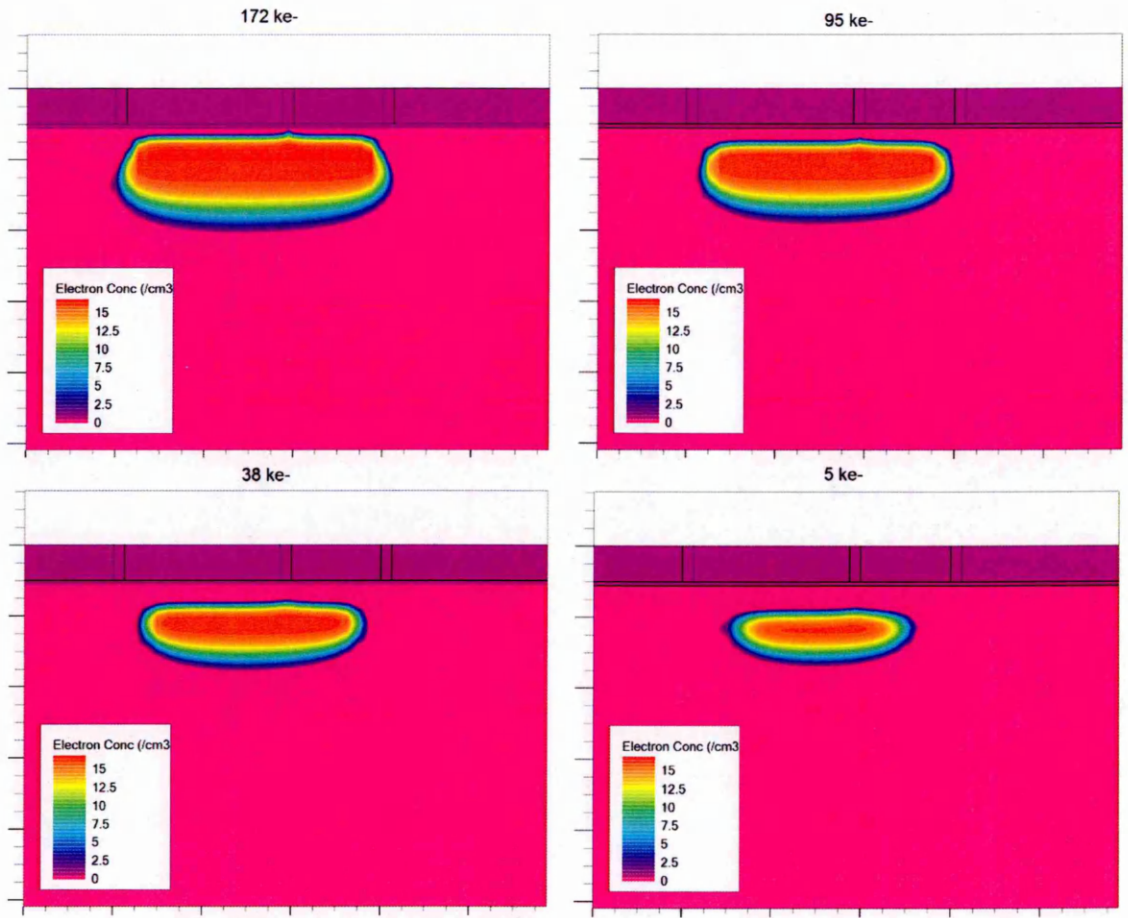


Figure 5.41: Charge packet (a.k.a. charge cloud) represented by electron concentration contour plot in the along channel dimension at a range of signal sizes, which gives an impression of how the charge packet distribution evolves. The electron concentration represented by contour colours is given over a logarithmic scale, so the value of 15, indicated by the colour red on the figure, refers to 10^{15} electrons/cm³.

The charge concentration can be plotted as a function of position across the pixel to show the charge packet distribution in any dimension. The distributions shown in Figure 5.42 give the charge packet in the x (along channel), y (substrate depth) and z (across channel) dimensions plotted for the charge packet over a range of signal sizes to indicate how the charge distribution changes. The plots of charge concentration in Figure 5.42 are used to determine the charge packet volume by measuring the extent of the charge packet dimensions once a cut-off density has been chosen to define the edge of the charge packet.

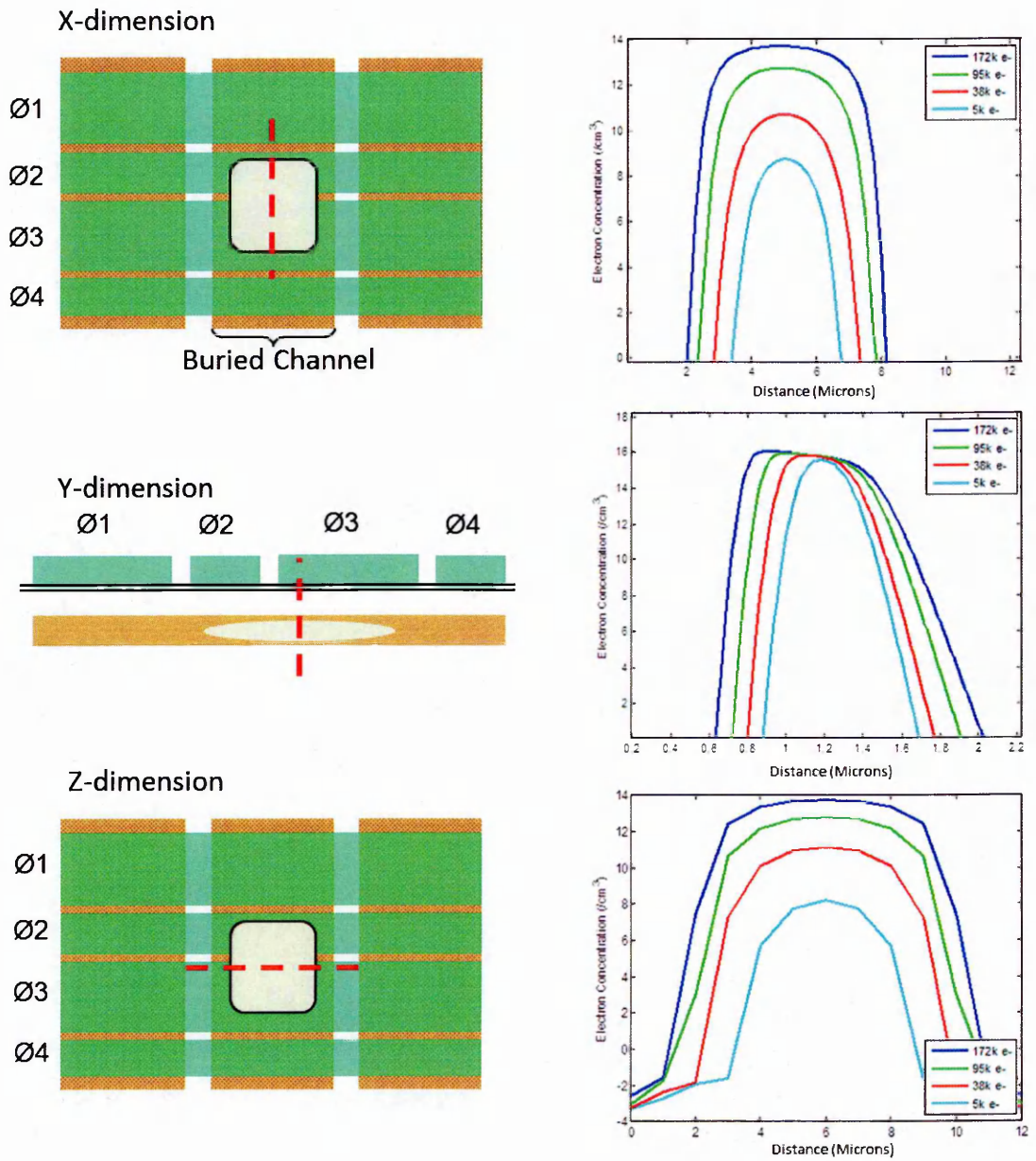


Figure 5.42: Example of charge distribution in each of the three dimensions x, y and z to give an impression of the charge packet evolution with signal size. These may be described by Gaussian distributions in each dimension, though the y-axis (electron concentration) of each plot is over a logarithmic scale.

The charge packet shows an approximate Gaussian distribution over a log-scale in each dimension. The maximum charge concentration in the buried channel is determined by the Gaussian doping profile and is $\sim 2 \times 10^{16} \text{ e-/cm}^3$, which is achieved in the high density core of the

charge packet but only at higher signal levels, evident in the charge concentration plots in Figure 5.42.

The distributions like those in Figure 5.42 can give an indication of the extent of the charge packet and the associated changes in volume and density as signal size increases. Owing to the fringing field at the edges of the active area, the charge packet does not exist as a solid mass of electrons at constant density. Instead the charge concentration reduces at the edges of the charge packet over a finite distance, where the concentration of electrons becomes small enough to be negligible. The effect of the fringing fields makes it difficult to define the volume which the charge packet occupies, but this problem is overcome by choosing a cut-off density at which the edge of the charge packet is defined.

5.2.1 Charge Trapping Effects

The main interest for the Euclid study is based around the interaction between charge packets and traps. The charge packet volume is measured by choosing a 'cut-off' density, beyond which the charge packet density will be too low to interact with any common electron trap configurations. In this way an effective edge can be assigned and the distribution measured in each dimension and a volume estimated.

Charge trapping is commonly modelled by Shockley-Read-Hall (SRH) theory which describes the probability of capture based on the density of a charge packet that comes into contact with a trap and the amount of time that charge spends in the vicinity of the trap. The SRH equations were introduced in Chapter 2, along with a table of trap parameters that are common in n-channel CCDs.

The SRH equations show that trapping is dependent on both charge density and the time which the charge packet is in the vicinity of the trap. As serial and parallel registers have differing transfer timing operations the density at which trapping is likely to occur differs between structures. Each trap type has a unique capture cross section (Holland, 1993), which allows them to be characterised, a single common trap type is used as an example in Figure 5.43 taken from

Table 2.1 in Chapter 2. Figure 5.43 shows that the capture probability differs between the two structures for a given charge density because of the differing readout speeds in the serial and parallel registers. The dwell time in the parallel register is of the order of 1×10^{-3} s, while the dwell time in the serial register is of the order of 1×10^{-6} s.

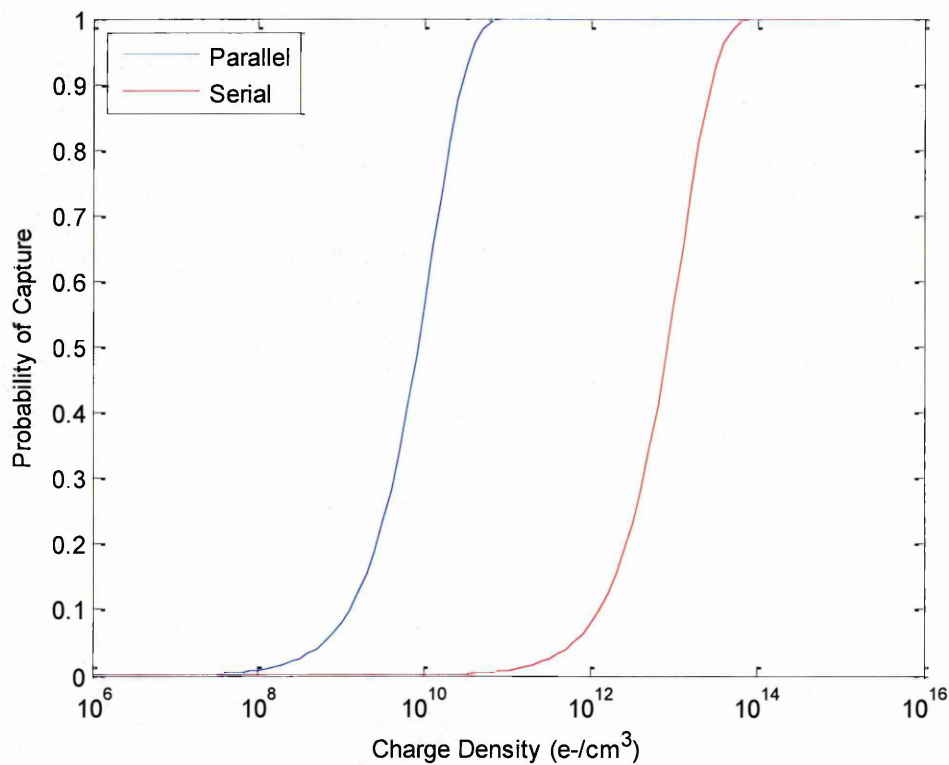


Figure 5.43: Capture probability as determined by SRH theory, given by Equations 2.1 and 2.2. It shows the probability of capture for the silicon-E centre trap ($\sigma=5 \times 10^{-15}$) (Hall, et al., 2012) over a range of charge densities based on the dwell time in both the serial (1×10^{-6} s) and parallel (1×10^{-3} s) registers.

The plot in Figure 5.43, compares the trapping probability across the parallel and serial registers for the silicon-E centre trap parameters, Table 2.1. The silicon-E centre has a capture cross section $\sigma=5 \times 10^{-15}$ (cm²) and the density of states in the conduction band is $N_t=1 \times 10^{11}$ (cm⁻³). The parameters of this trap are extracted from CCD analysis performed by Holland (Holland, 1993).

5.2.2 Charge Transfer Inefficiency from Packet Models

Shockley-Read-Hall theory illustrates the trapping probability versus charge density for a specific trap when the CCD is operated at a specific temperature. These equations can also be used to process the charge packet distribution, as modelled in each dimension using TCAD (Figure 5.42), to calculate the trapping probability as a function of position. Figure 5.44 shows the charge density distribution plots similar to those seen in Figure 5.42 alongside the same information after it has been processed using SRH to calculate capture probability. The new plots give the probability of capture for a specific trap, the silicon-E centre used to generate Figure 5.43, versus position. A dwell time of 1×10^{-3} s is used in the production of Figure 5.44 because this is reflective of parallel register timing parameters, as the charge density plots used in this example are from a pixel model. The probability of capture falls more sharply at the edges of the charge packet than with charge density, giving an approximately cuboid capture volume.

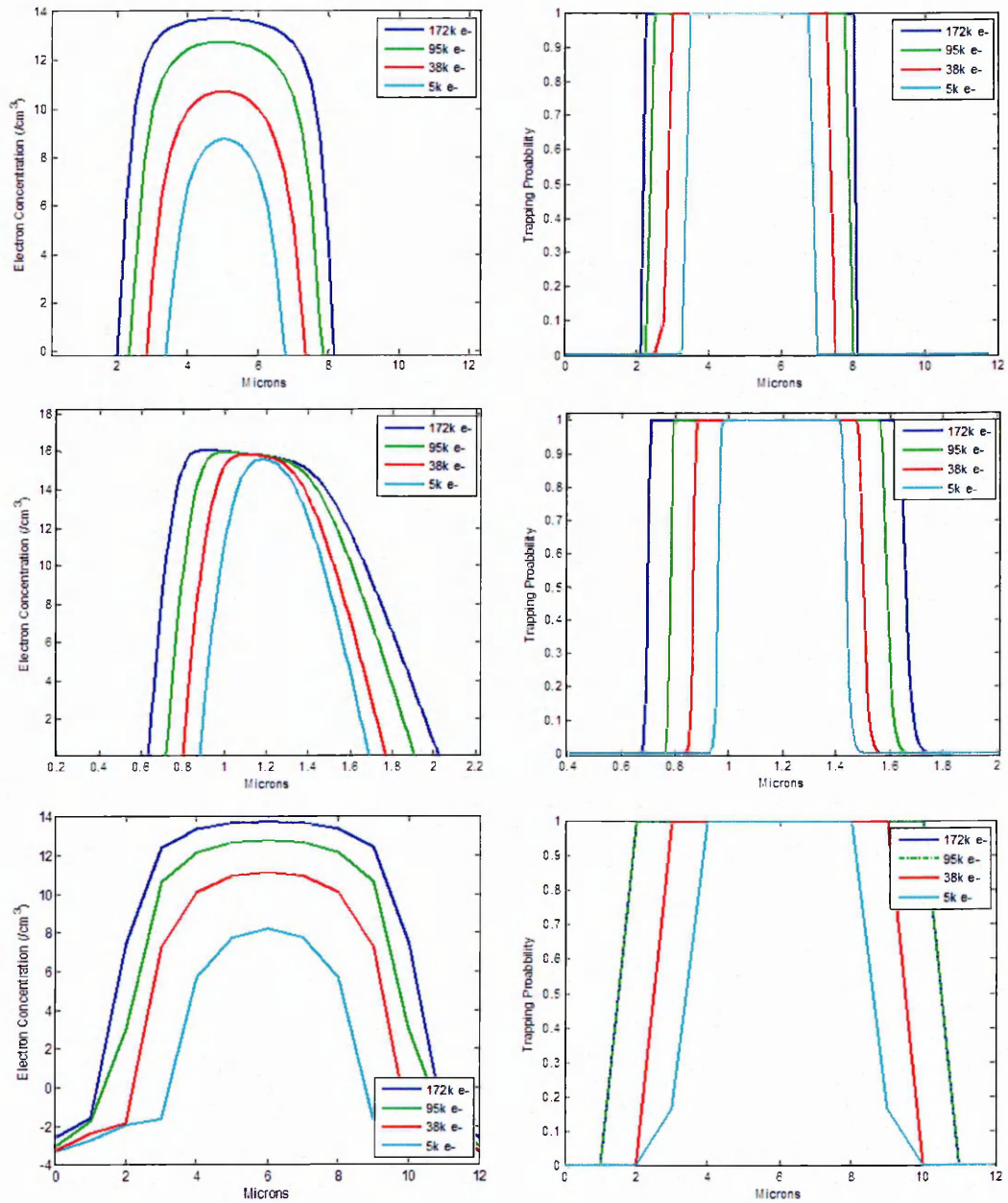


Figure 5.44: An illustration of how charge trapping equations used in SRH theory can be applied to the electron distributions and used to calculate the trapping probability versus position. The discrete nature of the solution mesh is evident in some figures, which will introduce a small error into future calculations.

The plots of capture probability, shown alongside charge density plots in Figure 5.44, show a rapid drop in probability, allowing a much better defined charge packet edge. There is only a fraction of a micron difference between positions which represent zero trapping probability and instantaneous trapping, even at small signal sizes. Again it should be noted that this is representative of one trap type, for a specific dwell time and temperature but the results are

similar for other traps. This technique has been used in the past, in 2D, by Hardy et al (Hardy, et al., 1998) when attempting to model CTE effects.

The probability of the specific trap being occupied by an electron from these packets is dependent on the trap position in the buried channel and the signal size. If the trap lies within the volume at which the probability of capture is 100% for the dwell time modelled, then CTE will be effected by that trap. Combining this data with expected average trap concentrations derived from radiation test campaigns, it is possible to model the expected CTE by calculating the percentage of filled traps versus unfilled traps, i.e. those that fall outside of the charge packet for a given signal.

5.2.3 Charge Packet Volume

As a choice of cut-off density can be made to define the packet edge, it is possible to estimate the volume which the charge packet occupies within a modelled structure. Where a data point, defined by the model mesh, does not lie exactly on the chosen cut-off density, linear interpolation is used to estimate the plot value at that point which introduces the errors seen on the volume calculation. There will also be some small systematic errors introduced by the discretised nature of the model mesh which were explored in Chapter 4.

By choosing a cut-off density to define the edge of the charge packet, part of the packet which is at a lower density and hence a lower probability of trap interaction is ignored. This is the only way realistically to compare like-for-like charge packet volumes across device structures. Once a cut-off density is chosen the dimensions of the charge packet can be determined in each dimension and it is then possible to estimate the volume which the charge packet occupies, Figure 5.45 shows the volume calculated for the pixel structure. The following sections present more volume information from a range of device models.

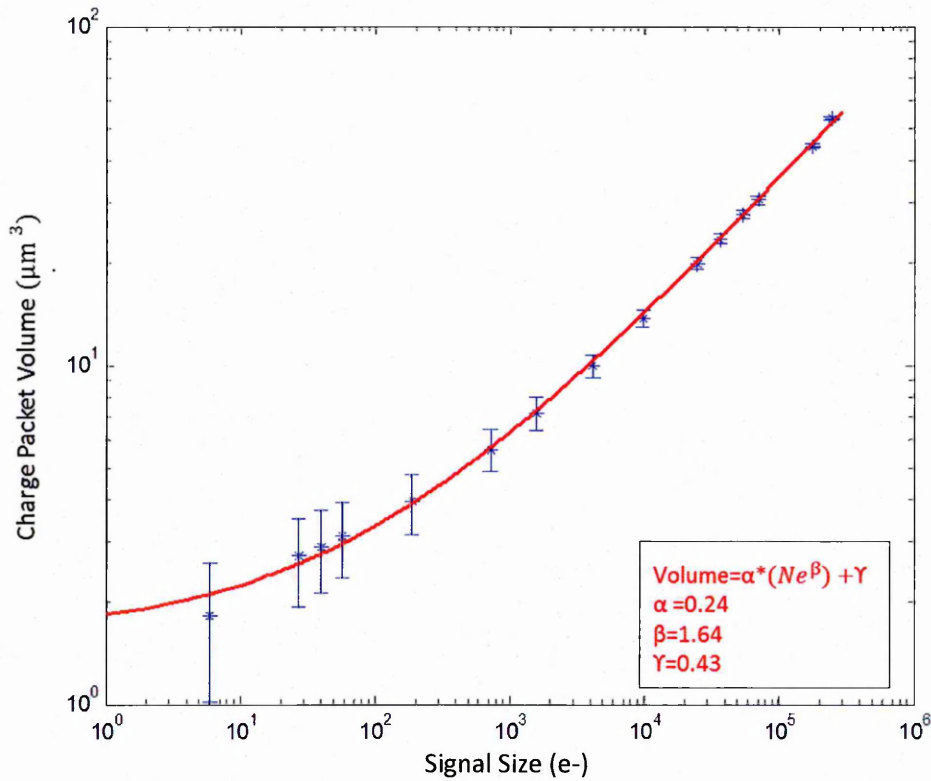


Figure 5.45: Signal vs. volume plot extracted from the Silvaco charge packet data for a $10^{10} \text{ e}^-/\text{cm}^3$ cut-off density in the Euclid pixel structure. The plot shows a characteristic power law trend as predicted by the interaction volume function at high signal, but is modified to fit the trend at small signal.

A plot of signal vs. volume with a cut-off density defined at $10^{10} \text{ e}^-/\text{cm}^3$ is given as a typical example in Figure 5.45. The distribution follows a general power law trend for larger signal sizes, which was predicted by the analytical CDM, but the data flattens off at small signal indicating charge packets have a larger volume relative to signal size. The lower average density at smaller signal levels indicated in Figure 5.45 is still sufficient for trapping to occur. The same data are shown later in the chapter for the register structures, and shows the volume is much larger at small signals, because the potential well is distributed over a wider area, producing a large area of equipotential for charge packets to occupy.

A function that fits the data has been applied, to give a simple mathematical description of how the charge packet volume changes with signal size. This function is very similar to that seen in the CDM model in Chapter 2, but with some modifications for the small signal trend.

The function used to fit to the data is given in the form:

$$\text{Volume} = \alpha N_e^\beta + \gamma \quad (\text{for } N_e \geq 1) \quad 5.10$$

α , β , γ are variables that change depending on the structural geometry being modelled and cut-off density chosen to represent the edge of the charge packet. In this function N_e is the signal size, which varies between small signal up to FWC, β is the power factor which determines gradient of the distribution on the log-scale plot, γ has a small effect on the gradient as it is the y-intercept value which determines the small signal distribution.

The function used to fit a trend line to the volume data is similar to the CDM equation, a good sign because the CDM is based on an analytical approach. The trend lines fitted to the data are useful for comparing the way charge packets behave in each model structure. However, it must be remembered that the trend line is not a physical description. Taken to the extreme small signal, the modified function effectively describes a fixed charge packet volume for a zero signal.

5.2.4 Effects of the Edge Cut-off

In the simulation output the charge packet is represented by a charge density distribution over log scale. At the edges of the distribution the charge density reduces over a finite distance until it becomes negligible. A density can be chosen with which to define the edge of the charge packet through the application of SRH theory allowing the volume to be estimated but this will change depending on the chosen cut-off density.

The cut-off density which represents the edge of the charge packet will affect the volume measured for any given signal size. Figure 5.43 gave an initial framework for choosing a cut-off value in the model data, based upon charge trapping theory. Here a comparison of the volume vs. signal plots show the effect of choosing different cut-off values on the charge packet parameters, as shown in Figure 5.46.

As higher cut-off densities are chosen, the calculated charge packet volume reduces, because more of the lower density fringe areas of the charge packet are ignored (Figure 5.46). Where the

signal size is small, the charge packet tends to be dispersed at a lower density over a larger area, as determined by the potential field. In some cases at very small signals ($<50\text{ e}^-$), the charge packet will not reach a high enough density to be measured using the more dense cut-off values.

The output from the pixel model, given in Figure 5.46, shows the effect that the cut-off density can have on the value of calculated charge packet volume. The pixel is the smallest structure modelled in this study. By contrast the same information is presented from the CCD273 and CCD204 registers, which have larger active areas (Figure 5.47 and Figure 5.48). These show the same general trends that can be described by Equation 5.10, but they are offset from the pixel data because charge is dispersed over a much larger area. As higher densities are used to define the charge packet edge, the data increasingly deviates from the observed trend shown in Figure 5.45, at small signal. The deviation occurs because the maximum density achieved by the charge packet will remain very low in larger structures, and in some cases will never reach the cut-off density used to define the charge packet edge, so either no volume data can be taken, or the volume measured will represent the very small high density “core”.

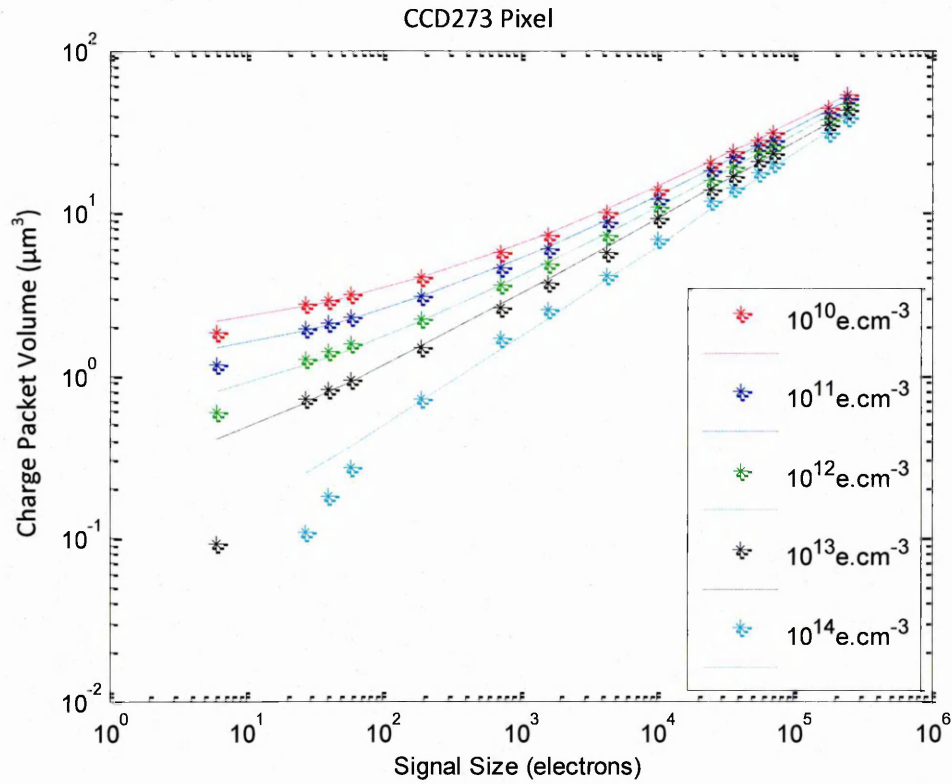


Figure 5.46: Charge packet volume is not only dependent on the signal size, but also on the way the edge of the charge packet is defined by using different cut-off densities to define the charge packet edge. This plot shows the variation of charge packet volume depending on the cut-off density used for the Euclid CCD273 image area pixel.

The problems encountered when attempting to measure the small signal charge packets with a high density cut-off are amplified in Figure 5.47 and Figure 5.48 because the charge packet is much more diffuse in larger structures, causing a drop in the measured volume at small signal. The CCD204 register model displays the poorest small signal volume data because it is the largest structure (Figure 5.48).

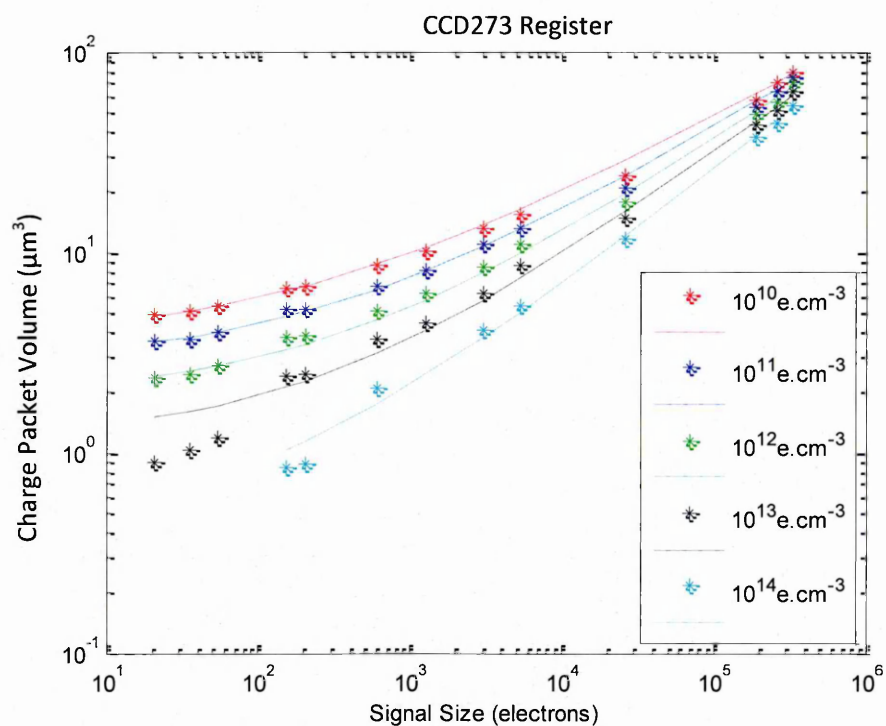


Figure 5.47: Charge packet volume is not only dependent on the signal size, but also on the way the edge of the charge packet is defined by different charge storage densities. This plot shows the variation of charge packet volume depending on the cut-off density used for the CCD273 register element.

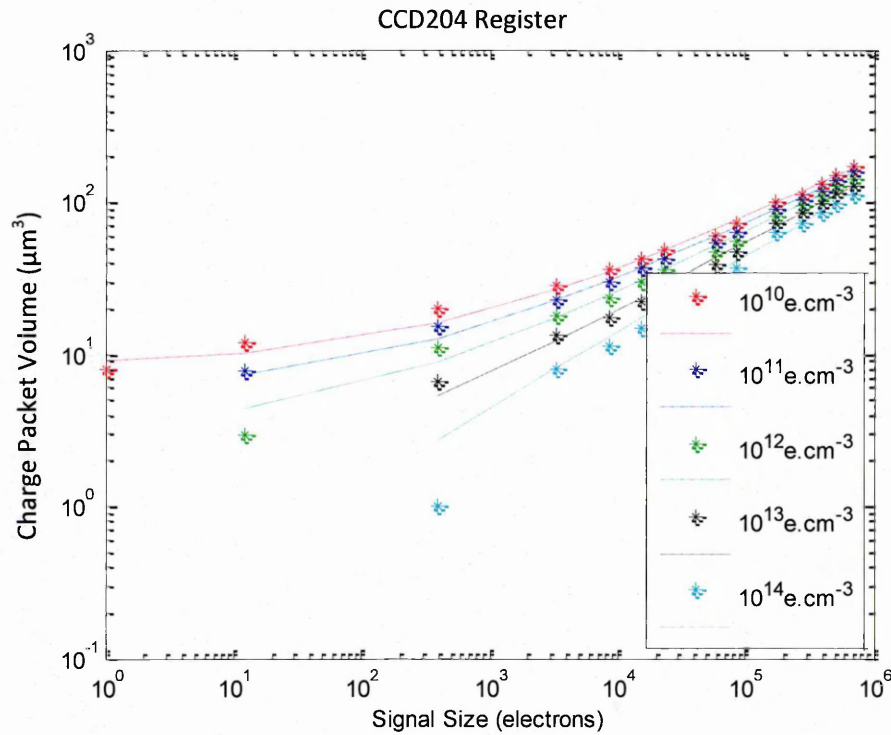


Figure 5.48: Showing the variation of charge packet volume depending on the cut-off density used for the CCD204 register, which is $\sim 2.5\times$ wider than the same structure in the CCD273. The larger volume occupied by charge in this structure indicates that this device will be more susceptible to radiation damage effects.

The data points in Figure 5.46, Figure 5.47 and Figure 5.48 are not evenly distributed in the x-axis because the charge packets at each simulation point is generated using a “beam” command, which simulates a beam of light of a certain wavelength and intensity incident on the CCD. The beam intensity is varied to introduce different signal sizes, so that the level of photo-generated charge which will be introduced to the model for a given beam command can only be estimated before the simulation is complete. Once a few data points are obtained, the value assigned to the beam intensity can be iterated around the values used previously to obtain signal values around those which have already been simulated.

Taking a single cut-off density it is possible to examine the change in fit line variables across each of the three structures, which indicates the change in charge packet distribution depending on geometry. By plotting the fit line variables against each device structure the aim is to find some pattern to the way charge behaves in the potential well depending on the volume which is

available to it. The plot in Figure 5.49 shows how the fit line constants change depending on the device model. These data are taken at the 10^{10} e-/cm^3 cut-off allowing for a direct comparison between the structures.

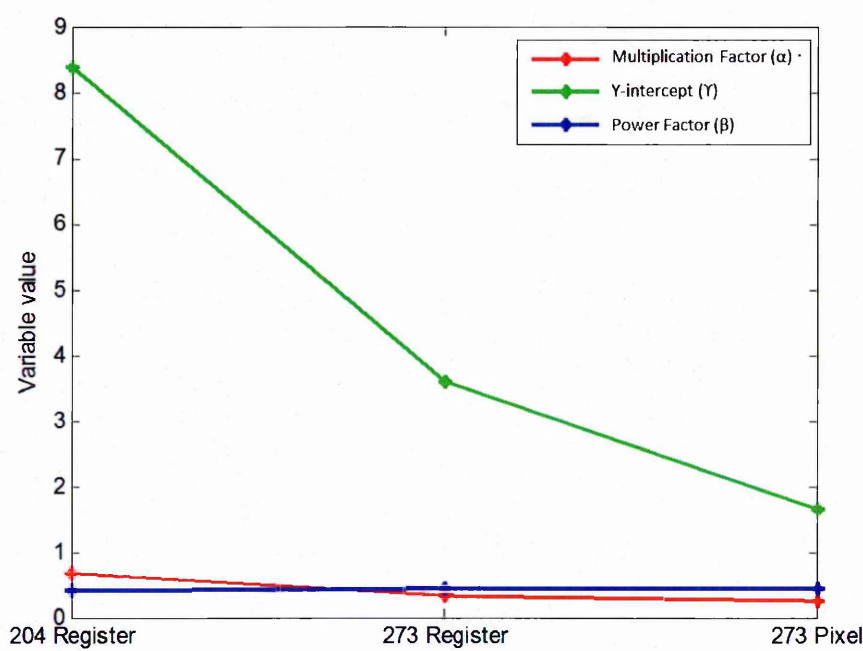


Figure 5.49: Comparison of fit-line variable values, from Equation 5.10, used to describe the charge packet volume trend across three model structures. These are from the signal-volume plots of each modelled structure (the CCD204 and CCD273) taken for a cut-off density of 10^{10} e-/cm^3 .

The data presented in Figure 5.49 shows how each parameter of the fit line, given by Equation 5.10, varies across each device model. The power factor refers to the β parameter, α is the multiplication factor and γ is the y-intercept referred to in Figure 5.49. The large change in the y-intercept across the structures indicates that the volume of charge packets at small signal sizes have a large variation depending on the structures size. Table 2 gives all of the variables attributed to the fit line (Equation 5.10) over a range of cut-off densities for each of the structures modelled.

	Cut off (e ⁻ /cm ³)	α	γ	β
CCD204 Register	10 ¹⁰	0.661	8.384	0.408
	10 ¹¹	0.607	6.170	0.410
	10 ¹²	0.450	2.060	0.426
CCD273 Register	10 ¹⁰	0.331	3.603	0.426
	10 ¹¹	0.189	2.795	0.465
	10 ¹²	0.101	1.923	0.508
CCD273 Pixel	10 ¹⁰	0.226	3.423	0.444
	10 ¹¹	0.197	2.641	0.453
	10 ¹²	0.243	1.643	0.430
	10 ¹³	0.198	1.019	0.442
	10 ¹⁴	0.155	0.446	0.456

Table 2: A list of values taken for the variables in Equation 5.10, from the lines of best fit to the signal-volume distribution calculations. Densities of 10¹³ and 10¹⁴ are omitted from the register entries because the charge packet does not reach these densities at small signal.

The value chosen for the cut-off density is important for these measurements. A low density cut-off value means that a large portion of the volume occupied by the charge packet will have a density that is too low to capture charge effectively at the charge transfer time constants. This is taken into account when choosing a cut-off density for CTE models. A range of data are presented here for completeness.

Where the density used to define the charge packet edge is too high, the charge packet may not reach this density at smaller signal sizes making the volume measurement impossible. The fit line is used to describe the evolution of charge packet volume with signal size as a simple mathematical function, which allows charge packet volume to be estimated for a given signal level. The signal-volume trend appears to be very similar across each structure, with additional “y-intercept” offset for larger structures as shown in Figure 5.47 and Figure 5.48.

5.3 Comparing Charge Packet Models

Both the CDM and Silvaco models described so far are derived in different ways. The Silvaco models are calculated based on well tested and widely accepted field theory as derived from Maxwell's and Poisson's equations, whereas the CDM function is used to describe some of the effects observed in tests carried out on CCDs over various CTI modelling campaigns (Massey, 2010) (Prod'homme, et al., 2011). This section compares the models to note the differences between the predictions about the charge packets derived from tests, and the charge packet that the semiconductor field equations dictate.

The limitations of both the Silvaco charge packet modelling and the interaction volume function have already been explored in detail. This section compares the two modelling methods directly, over the typical signal range expected during the Euclid mission. The Silvaco simulations have shown that the charge distribution differs depending on the size of the device structure. By contrast the interaction volume function does not take any physical device parameters into account, but can be calibrated for specific devices by choosing the β parameter, which determines how the charge packet volume changes with signal size.

The interaction volume function is compared to the Silvaco data by fitting a line using a non-normalised version of the interaction volume function ($\text{Volume}=\text{Signal}^\beta$) to the charge packet volume data calculated from the Silvaco models. This gives a value for the fitting parameter, β , in the interaction volume function (which presents the best match to the Silvaco model data and is between 0 and 1). The line derived from the CDM function is plotted along with the fit-line which was developed for the Silvaco data, Equation 5.10 for a direct comparison.

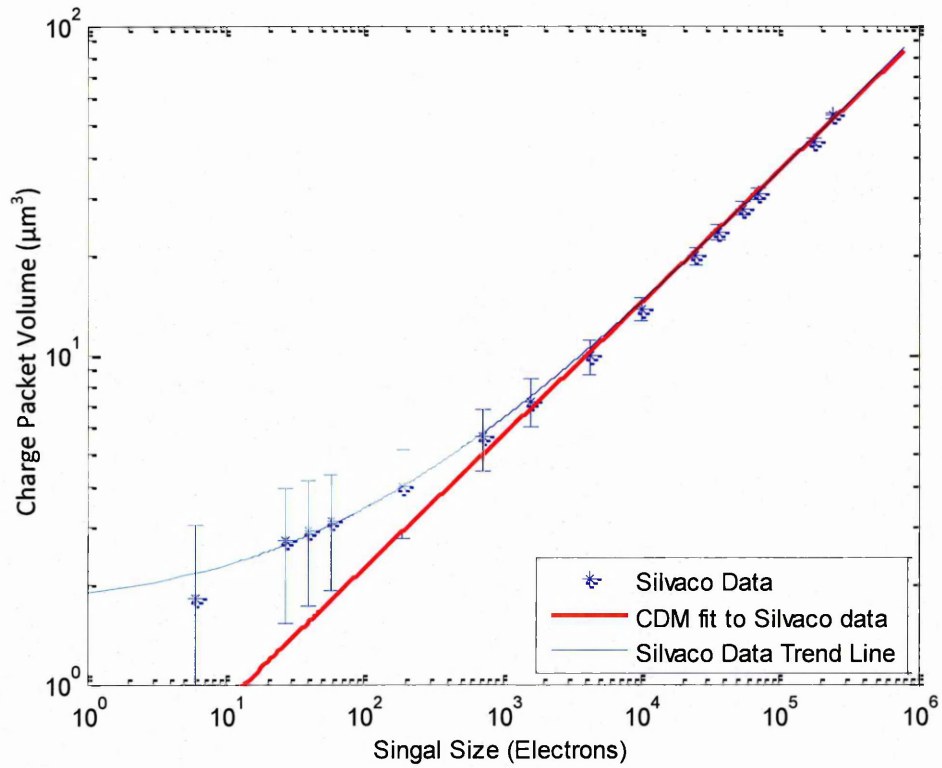


Figure 5.50: The fit line used to describe the charge packet volume for the CCD273 pixel at a 10^{10} e-/cm^3 cut-off is compared against the CDM function which is used to find a 'line of best fit' to the Silvaco data. The CDM function provides a reasonable fit at larger signal sizes, but diverges from the volume trend at smaller signals.

The CDM function comes very close to the trends predicted by the Silvaco models at higher signal levels, perhaps unsurprisingly, because the CDM is based on analytical analysis. However, the main difference between the CDM function and the trend line fitted to the Silvaco data comes at small signal (Figure 5.50) the signal range where the CDM function failed to accurately predict observations in Gaia. The fit line used to describe the signal-volume distribution calculated from the Silvaco models tends to intercept the y-axis at a value larger than zero, producing a much larger charge packet in relation to signal size at small signals. It is hoped that this will produce better predictions of device functionality.

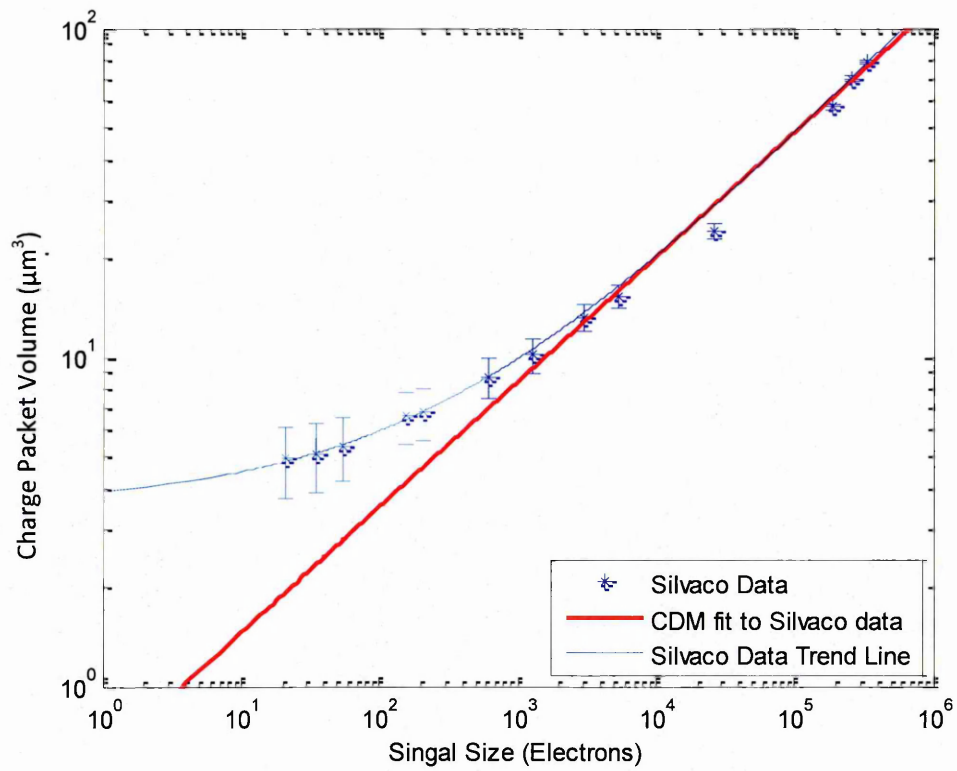


Figure 5.51: The fit line used to describe the charge packet volume for the CCD273 register at a 10^{10} e-/cm³ cut-off is compared against CDM function which is used to find a 'line of best fit' to the Silvaco data. This is a larger structure, causing the variables of the CDM function to differ from the pixel. The small signal fit is poor as in the pixel trend.

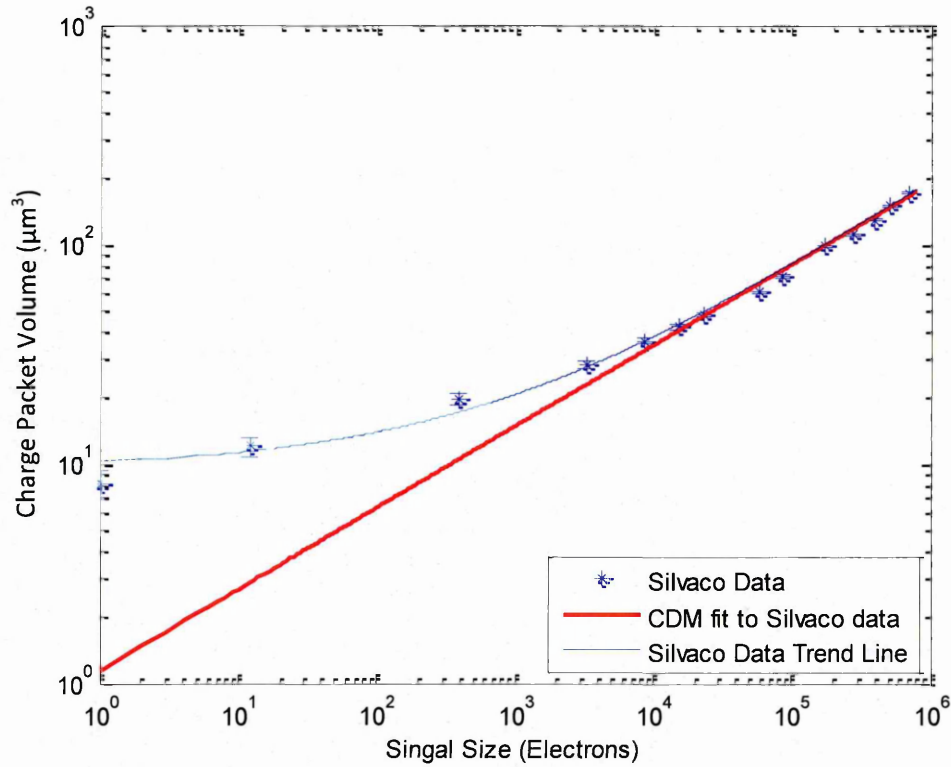


Figure 5.52: The fit line used to describe the charge packet volume for the CCD204 register defined using a 10^{10} e-/cm^3 cut-off is compared against the interaction volume function which is used to find a 'line of best fit' to the Silvaco data. Fitting the CDM function to the small signal data points appears to get progressively worse as the structure size increases.

The charge packet volume measured in the Silvaco models is based on the physical characteristics of the CCD, such as gate geometry, doping and applied voltage. Thus the charge packet is different depending on the modelled device structure. The cut-off density chosen to define the edge of the charge packet affects the measured volume, and in the case of small signals the charge packet may be dispersed over a large volume, making measurements difficult. With such modelling, charge packets at signal sizes down to tens of electrons are possible. Therefore the description of the charge packet at signal sizes smaller than this relies on the extension of the trend line.

It is reassuring that the general large signal trend tends to agree between the Silvaco model data and the CDM function, given the heritage which comes with the CDM function from observable effects in the Gaia data. Where the interaction volume function has given poor insight at small

signal, the fit line equation used for the Silvaco data offers an alternative which will be explored further in later chapters.

The previous figures comparing CDM model to the Silvaco charge packet data perform the comparison over the entire signal range. As the CDM is derived analytically several attempts have been made to determine the β line fitting parameter from Gaia test data (Short, et al., 2012). Unfortunately many of these studies have given conflicting β values. This is most likely to be caused by testing the Gaia devices at specific signal level ranges. It is evident from Figure 5.50, Figure 5.51 and Figure 5.52 that fitting the CDM model to smaller signal ranges will result in a different β parameter than if the measurements are made over intermediate or higher signal levels.

5.4 The Effects of Device Geometry

The following sections outline studies that were performed as part of the Euclid CCD development, which took place alongside the development of these Silvaco device models. Initially the models were used to predict the relative improvements in performance which might be expected by changing the serial register geometry between the CCD204 and the CCD273.

The redesigned CCD204 register utilised in the CCD273 is implemented with a reduced channel width. It is assumed that by confining the charge packet to a smaller area, it will interact with fewer charge traps and improve charge transfer efficiency, as seen with the use of the supplementary buried channel in Gaia. This section compares the charge packet volume calculated from the Silvaco device models to analyse the effect which the register redesign has on the charge packet.

If assumptions of trap interaction based on charge packet volume prove to be correct the difference between the volume calculated in the register models of the CCD204 and the CCD273 should show a similar trend to the difference in CTE observed between these devices. This comparison is achieved by taking the 10^{10} e⁻/cm³ threshold, so that the model extends down to small signals. This is important because the small signal characteristic of the distribution varies

greatly across the structures and can be missed at higher cut-off densities. Small signal is also the area of interest as the expected signal range for the Euclid mission in the region of hundreds of electrons. These data are plotted for each of the structures modelled in Figure 5.53, enabling a direct comparison.

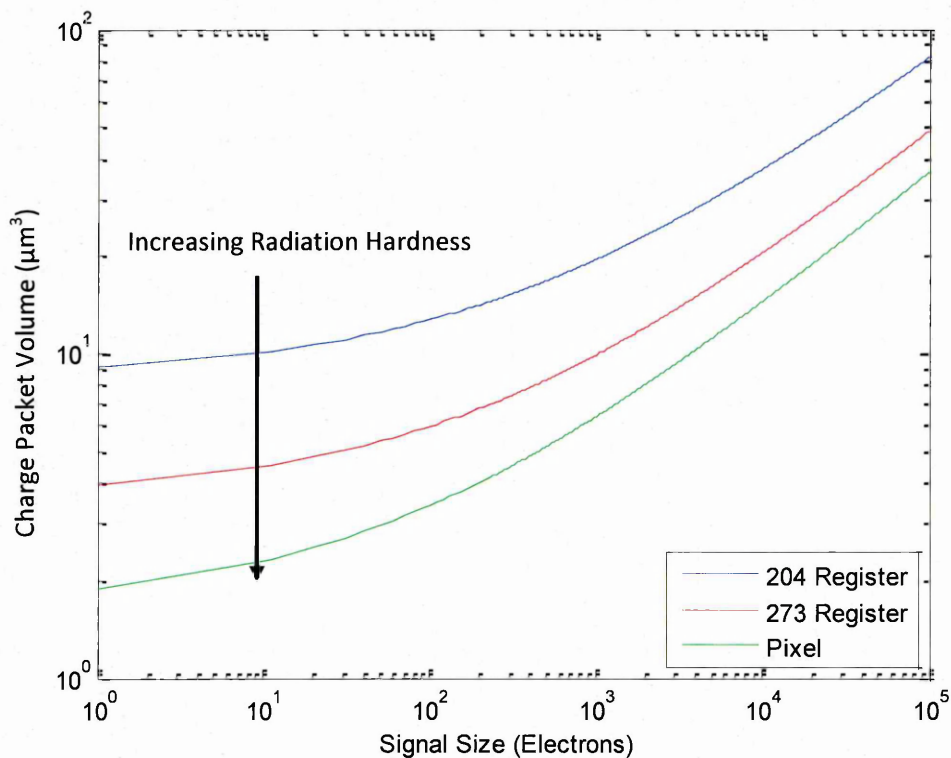


Figure 5.53: Comparison of the charge packet volume in each of the structures modelled. These are taken at a 10^{10} (e-/cm³) cut-off density, so that the comparison is like-for-like across the structures. Charge is dispersed over a wider volume in the larger structures increasing the volume measured for a given signal size. Larger volume charge packets will result in more trap interactions per signal charge thus reducing radiation hardness.

Figure 5.53 shows that the way devices are manufactured has a large influence on the charge packet distribution. The volume that the charge packet occupies is dependent on signal size and channel doping, but also pixel geometry, with charge packets taking up more space in larger structures, with lower average densities. As bulk traps are assumed to have a fixed, uniform density, smaller charge packets will interact with more traps per electron of the charge packet,

causing the disproportionately high CTI at small signals usually reported in CCDs (Hardy, et al., 1998).

The SRH equations presented in Chapter 2 showed that the trapping probability is dependent on the transfer time as well as charge density, capture cross section and temperature. As the serial and parallel registers of a CCD are generally operated under different timing regimes, because the charge transfer between the parallel and serial registers is delayed by each serial readout, the density at which trapping becomes likely will differ between the two structures and this should be taken into account when calculating the volumes of the charge packets in the two structures.

The CCD273 and CCD204 share the same pixel architecture, so charge distribution will be the same in both devices. However the serial register has been redesigned, which makes it possible to compare the volume distributions between the two devices. The change in channel width between the CDC204 (50 μm) and the CCD273 (20 μm) serial registers is a factor of 2.5. Figure 5.54 shows that the change in charge packet volume for any given signal size is not x2.5 between the two registers. By calculating the ratio difference between the volumes of charge packets in the register structures for each given signal size it is possible to track the difference between the structures.

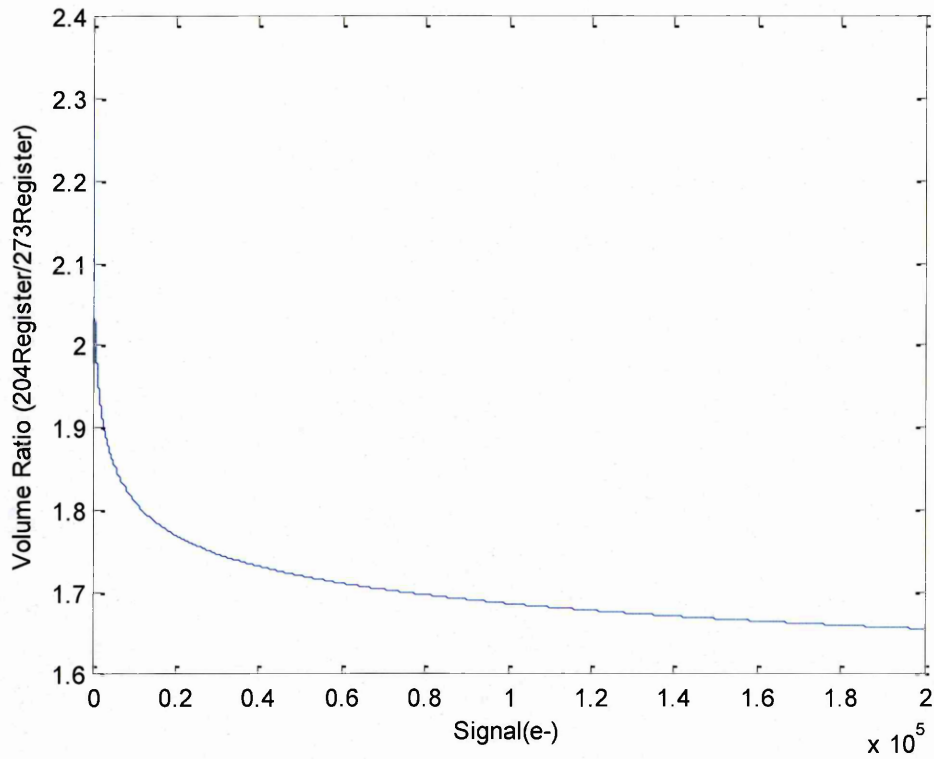


Figure 5.54: Direct comparison between the charge packets modelled in the CCD204 and the CCD273 registers. This is achieved by calculating the ratio difference in volume between the trend lines plotted in Figure 5.53. The difference in the volume occupied between the structures is larger at small signal, but levels off at ~ 1.7 where signal is greater than $\sim 1 \times 10^5$ e $^-$.

The comparison between the CCD204 and the CCD273 registers presented in Figure 5.54 is the ratio difference between the fit lines used to describe the charge packet volume at a single cut-off density of 10^{10} e $^-$ /cm 3 . At the smallest signals the difference in charge packet volume between the CCD273 and the CCD204 registers approaches the difference in active area, but over most of the signal range the difference in volume is much smaller than the x2.5 difference which exists between the electrode geometry of the two devices.

In smaller structures, the fringing fields take up a much larger proportion of the active area, causing the area available to the charge packet to be small. In larger structures, the fringing fields around the edges of the active area are much smaller as a proportion of the structure size, resulting in larger charge packets, especially at small signal sizes. Once the charge packet passes a particular signal level, the charge packet volume is determined by the fringing fields at the edges

of the storage area and once this occurs the increase in charge packet volume with signal level takes on a very similar trend across each structure, which can be seen in Figure 5.53.

The relationship between the charge packet and the potential well dictates the shape of the trend when plotting the volume ratio in Figure 5.54, with a large difference at small signal levels, reducing as the signal level increases to some constant value. As the charge packet volume does not have a directly proportional relationship with the signal size or the structure size, the change in charge packet volume between the two registers is not a simple x2.5 difference.

5.5 Supplementary Buried Channel

The information extracted from the charge packet models can be useful in evaluating the effectiveness of design changes for radiation performance, as seen in the previous section. During the development of the Euclid CCD, the effects that an supplementary buried channel (SBC) might have on device performance were studied. This section looks at the introduction of a SBC into the Euclid pixel model, similar to that which is present in the Gaia pixel (Seabroke, et al., 2013). The SBC was used in the Gaia pixels to improve parallel CTI because of the large pixel geometry (it had a 30 μm wide channel). As Euclid pixels are already very small in comparison (12 x 12 μm) and readily achieve their CTE specifications, there will not be an SBC included in the design. However, it is interesting to note the effect an SBC has on the signal-volume function and the effect that the position of the SBC within the pixel can have on the charge packet.

A supplementary buried channel is an area within the buried channel that is more highly doped than the buried channel itself. It forms a secondary channel, usually just a few microns across, where charge is confined at small signals. When the SBC reaches saturation, charge will spill into the wider buried channel as the signal size increases.

The Silvaco models were used to assess any possible impact the introduction of a buried channel might have on the charge packet volume, and therefore on CTI performance. This required only minor modifications to the doping specifications in the model development environment, and also to the solution mesh, due to a new area of interest and doping junctions within the buried

channel structure. Two positions for the SBC are evaluated. The first SBC position to be evaluated is at the edge of the buried channel, adjacent to the channel stop, which is the most likely position from a manufacturing point of view and reflects the SBC position in the Gaia pixels. The second analysed SBC position is in the centre of the buried channel.

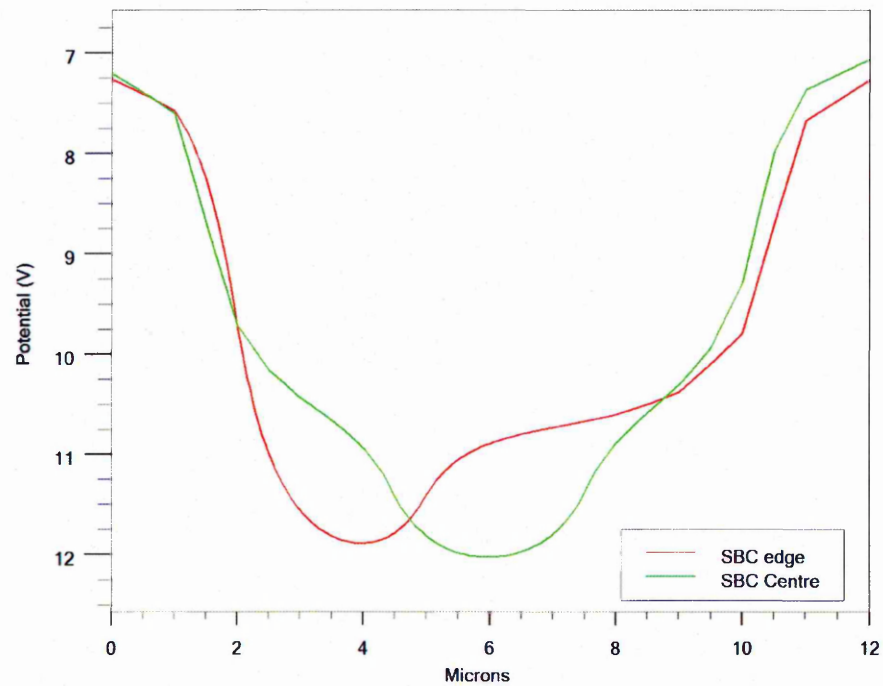


Figure 5.55: The potential well formed in the across channel dimension of the Euclid Pixel when an SBC was present.

Two positions for the SBC were investigated for the reduction in charge packet volume at small signal, where the SBC is positioned at the edge of the buried channel and in the centre.

The SBC is manufactured by counter-doping sections of the buried channel to reduce the net-dopant concentrations in those areas. This process leaves areas that are not counter doped at the original doping concentration (i.e. at a higher doping concentration than the counter-doped sections). The SBC causes an area of higher potential to form within the potential well during operation (Figure 5.55) where small signal charge packets are stored. The models are made to mimic this manufacturing method, so areas of constant p-type doping concentration are introduced to counter dope sections of the n-type buried channel region. The doping

concentrations for the buried channel and the width of the SBC region used here are an approximation based on values used in the Gaia devices.

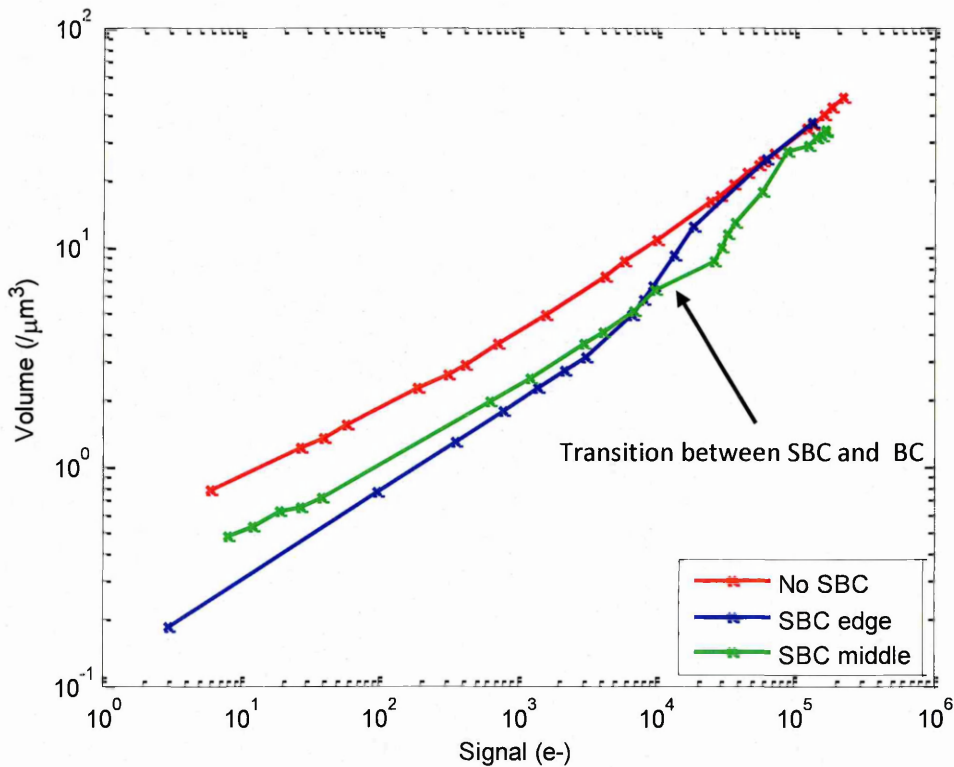


Figure 5.56: Variation in charge volume with signal size determined for the Euclid pixel with and without a supplementary buried channel, these plots are taken using the $1\text{E}10\text{ (e-/cm}^3\text{)}$ cut-off density. The extra fringing fields introduced by the SBC reduce the accuracy of the volume calculation at the transition between SBC and BC.

Figure 5.56 shows the maximum SBC capacity as a 'knee' in the distribution at $\sim 1 - 3 \times 10^4\text{ e}^-$ depending on the SBC position, which indicates electrons spilling from the SBC into the wider BC causing a sudden increase in the charge packet volume. This knee occurs at a higher signal level when the SBC is centrally positioned indicating a larger charge capacity in the centrally positioned SBC. Looking back at the comparison of the potential wells for each SBC position in Figure 5.55, the central SBC appears to have a larger potential well, which indicates that more charge can be stored in it before saturation.

Both SBC models show a smaller charge packet volume at small signal due to the restriction of charge in one dimension. Where the SBC is positioned at the edge of the buried channel the volume occupied is smaller than the packet volume when the SBC is positioned in the centre of the pixel, with a potential for a reduction in charge-volume up to 2x at small signals, improving radiation performance of the detector.

This analysis shows that the charge packet is confined to a smaller volume at small signals when compared to the SBC-free pixel. The charge capacity of the SBC is affected by its positioning in the pixel, where positioning at the edge of the structure introduces effects from the fringing field which reduce the well capacity. But it also shows that once the SBC becomes saturated the volume rapidly expands to fill the wider buried channel translating to virtually no change in storage volume at high signals.

The volume distributions show some variation from a smooth distribution over signal size where an SBC is present because the cuboid approximation applied to calculate charge packet volume does not reflect the charge packet when the SBC is present, making some approximation necessary. However it is generally accepted that the performance gain from the use of an SBC will be much smaller than the performance gain from calibrating the transfer rate and using CTI mitigating techniques (Hopkins, et al., 1994). The SBC was not adopted into the Euclid CCD design because of the small size of the pixels and the effects of the SBC on the charge packet and trapping, which make calibration and correction techniques more difficult to implement. More particularly, the transition region where charge spills into the wider buried channel from the SBC would require a larger calibration effort.

5.6 Conclusions

The Euclid CCD273 uses small pixel geometry, coupled with a narrow readout register in an attempt to achieve high CTE performance under irradiation. It is theorised that the volume occupied by the charge packet is related to charge transfer efficiency through interaction of the charge packet with traps which are distributed in the buried channel. By reducing the geometry of the readout register in the CCD273 the designers hope that the charge packet will be restricted to

a smaller area and will interact with proportionately fewer traps, thus improving CTE. The charge packets are modelled here over a range of signal sizes. The models are produced in Silvaco TCAD and are based on device geometry so that the relative change between the CCD273 and the CCD204 can be calculated to try and predict the improvement between the two devices.

The Charge Distortion Model (CDM) describes the two model methodologies used in the Gaia CTE campaign. These models take no account of device architecture but are calibrated against empirical observations made during device testing. An optimised signal-volume model is presented that is derived from the charge distributions modelled in the Silvaco simulations. Silvaco models are directly related to the physical structures of the CCD and so present a much clearer view of the evolution of the charge packet. In some cases at small signal the charge packet may not reach a density that can be measured using the methods described – in these cases the plots can be incomplete and rely on the extension of the fit line beyond the value calculated from the models.

A mathematical function similar to the interaction volume function, but with some new parameters, is fitted to the signal-volume data extracted from the Silvaco models to describe the evolution of the charge packet as signal size increases. This fit varies between structures with differing geometries and is affected by the cut-off density used to define the edge of the charge packet. The charge packet volumes described by the interaction volume function tend to match Silvaco output at large signal, but there is a large divergence at small signal when the fit is made over the entire signal range.

The Silvaco models have shown that the charge packets are confined to a finite volume determined by the lateral extent of the potential field which is controlled by the gate geometry, and the potential well that forms across the depletion region. The mutually repulsive nature of the charge carriers acts against the potential well which confines the charge packet, which results in a dynamic arrangement of electrons best described by a charge density distribution. Charge packets with a small signal level tend to occupy a disproportionately large volume, and this tends

to vary depending on the structure's geometry, with larger structures showing larger volumes, at lower average densities, for the same signal size. A similar effect is present in results published to measure CTI over a range of signal sizes (Hardy, et al., 1998), showing CTI is disproportionately large at small signals. With charge packets occupying larger volumes as a proportion of signal size at small signals there will be more traps per charge carrier, increasing the likelihood of a trap interactions.

The charge packet tends to be more dispersed in larger structures because the potential well reaches its maximum channel potential and is less likely to be influenced by the fringing fields at the electrode edges. The charge packet tends to be a distribution of charge with a higher density in the centre and gradually reducing over a finite distance towards the edges, resulting in the typical 'charge cloud'. As signal size increases so do both the density and volume of the charge packet until full well capacity is reached.

The Gaia mission attempted to mitigate the CTE problem by introducing an SBC into the parallel registers. The SBC was introduced because the Gaia pixels are much larger than those used in Euclid, $\sim 30 \mu\text{m}$ across. In the last section of this chapter, the effects of a hypothetical SBC in the Euclid pixel are explored, although the inclusion of an SBC is unlikely due to the already small size of the Euclid pixel. The models showed that the SBC tends to improve CTI at small signal levels, until the SBC becomes saturated and charge spills into the wider buried channel. While an SBC does reduce the volume at small signal, the volume at large signal is relatively unaffected and its presence increases the complexity of any corrections which are applied to the data.

5.7 Summary

This chapter has shown how device models can be interpreted and used in determining the behaviour of charge within a CCD. Device models offer a unique insight into the distribution of charge, especially at small signal which has been lacking in previous studies based on the analytical analysis of charge packets such as those performed for Gaia based on the CDM. The charge packet information extracted from device models broadly agrees with analytical models but offers a new insight into behaviour at small signal. This analysis can potentially offer improved

predictions of device performance and aid in data analysis from the detectors as well as improving correction techniques.

This work has demonstrated that the CCD273 is more radiation hard than the CCD204 thanks to its redesigned serial register. Further improvements to the CCD273 are also possible, as shown in the latter sections of this Chapter, offering a factor 2 improvement in radiation performance at small signals. These improvements were not adopted by the project team due to the complexities of calibration that would be required to correct the resulting images, (i.e. if a supplementary buried channel had been included in the design).

Chapter 6: Model Verification: Factors affecting FWC

Full well capacity (FWC) is a device parameter that describes the maximum amount of charge that can occupy a single pixel cell before saturation occurs. At the saturation point, charge will spill from the original pixel into neighbouring pixels, a process known as blooming, which occurs along the buried channel. This makes FWC an extremely important device parameter because a particularly bright light source may saturate a number of neighbouring pixels and cause blooming along columns that would mask any other information held in these areas. The blooming tail also causes distortion in images, which is especially important in Euclid where very accurate measurements of the shapes and positions of galactic objects are sought. The CCD273 is designed with a large FWC, ($\sim 1.9 \times 10^5 e^-$) in the image area compared to the expected signal level ($\sim 1 - 5 \times 10^2 e^-$), which should prevent blooming for all but the brightest objects.

This chapter explores the FWC measured in both simulation and laboratory based experiments on a CCD204 test camera (Figure 6.57). The CCD204, described in Chapter 3 is used because it shares many design characteristics, including pixel design and doping parameters, with Euclid's CCD273.

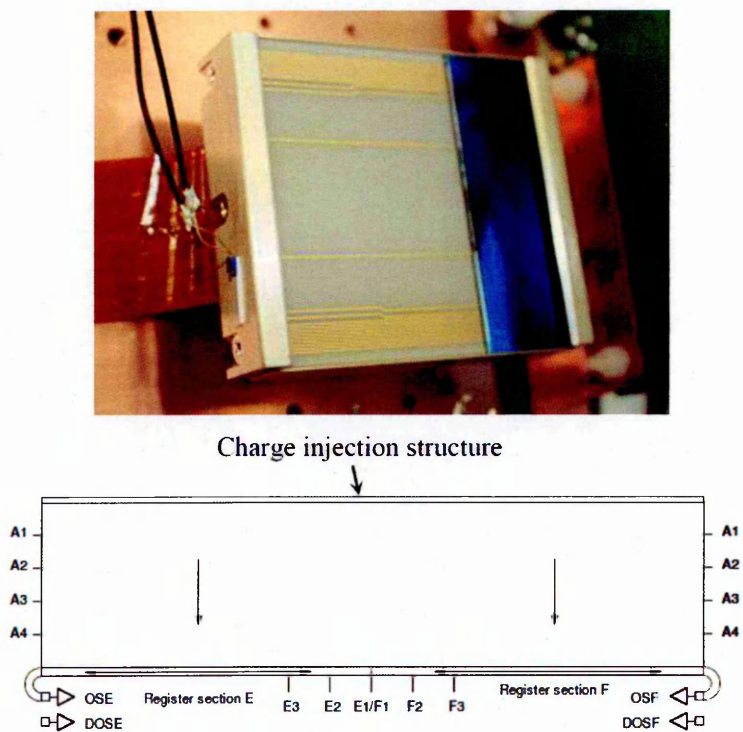


Figure 6.57: Image and schematic of the CCD204 test device used to produce the results presented in this chapter.

The results are taken from the CCD204 test device and take the form of a photon-transfer analysis, which makes it possible to investigate several device parameters, including FWC, through the relationship between the mean signal level and the corresponding RMS noise on the signal.

Full well capacity is a fundamental limit to device performance because it describes the signal size when a pixel or register cell becomes saturated and charge begins to spill, or bloom, into a neighbouring structure. It is directly affected by several device parameters including:

- Device doping.
- Pixel geometry: where a physically bigger pixel results in larger potential wells, meaning the pixel can hold more charge – thus higher FWC is achieved.
- Biasing conditions: where an optimum biasing condition exists to achieve the maximum FWC, without blooming or surface contact, as seen in Chapter 3 (Janesick, 2007).

Generally, blooming occurs along the parallel registers, spilling across the inactive electrodes that form the potential barrier normally preventing the charge from escaping the potential well. Occasionally, blooming may occur across the channel stop regions (i.e. across rows) that separate the parallel columns, but devices are usually designed in such a way to make the potential barriers presented by the channel stop regions larger than the potential barriers of the inactive electrodes causing charge to preferentially spill along the parallel channels.

FWC is used for model verification here, because it relies on a wide range of device parameters and it is directly related to the charge storage mechanisms, which are an important part of the Euclid investigation presented in this thesis. Agreement between modelled FWC and that measured in the CCD204 test camera should suggest accurately simulated charge storage characteristics. However, as has already been observed in the FIBSEM results there may be an over-etch problem during manufacture which results in at least one smaller than expected gate electrode and this may cause problems when attempting to match simulation results to measurements. This is investigated further during this chapter to ensure any deviation from

design in the test device does not disproportionately affect confidence in the models which currently take no account of manufacturing variation.

6.1 Photon Transfer Curve

Mean variance analysis (also known as the Photon Transfer Curve (PTC)) was first developed to assess and characterise solid state camera systems in the 1970s by Janesick (Janesick, 2007). The basic photon transfer method requires no special equipment, only a camera system and computer. The data that are processed are the mean signal and the variance about that mean, the RMS noise. This data acquisition provides a wealth of information about the camera system and detector. Making it possible to measure read noise, dark current, full well capacity, sensitivity, dynamic range, camera system gain and linearity (Janesick, 2007). However, a properly processed PTC should only contain shot noise limited data, giving the gain of the camera system and the FWC.

The total measured noise varies with signal size, and different noise sources in the camera system each have their own identifiable characteristics by becoming dominant in different signal ranges. There are three noise sources that are relevant to this work; these include read noise, photon shot noise and detector fixed pattern noise, which are labelled in Figure 6.58 and described in detail in Chapter 3. The fourth noise regime present in Figure 6.58 is characteristic of the full well capacity and is defined by a drop in the measured noise due to an averaging effect when the charge blooms between pixels. It is the location of this regime which is the ultimate goal of these measurements.

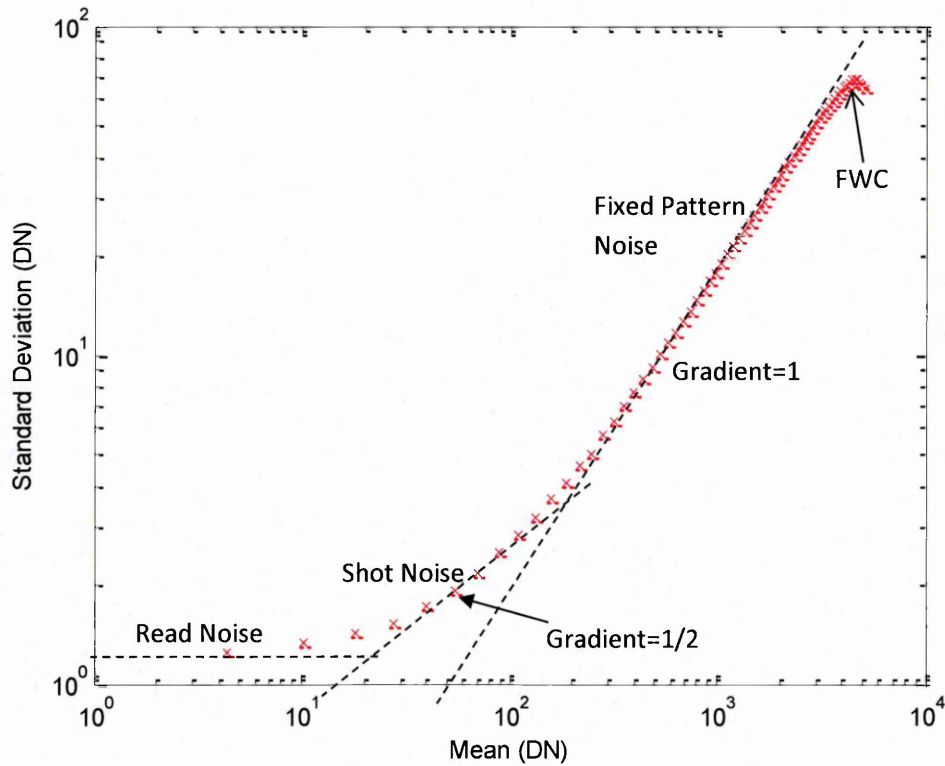


Figure 6.58: The classic PTC produced from unprocessed data using a region of interest in the CCD204 image area. Each of the different noise regimes is labelled. The axes are given in units of digital numbers, the conversion between DN and electrons is covered in a later section of this chapter.

6.2 Noise Regimes of the Photon Transfer Curve

6.2.1 Read Noise

Read noise is caused by the readout electronics and is dominant at small signal (Figure 6.58). It is defined where the gradient of the PTC tends to zero, which shows that read noise is independent of signal size and defines a minimum resolution for the camera system. Read noise can be contributed to by source follower noise, sense node reset noise and ADC quantisation error (Janesick, 2007).

Reading out more pixels than actually exist in the CCD creates an area of overscan in captured images. These are virtual pixels, shown in Figure 6.59, which give a measurement of the zero charge level. As the virtual pixels are exposed to the same readout electronics, any noise measured in these pixels can be attributed solely to the readout electronics and the values

measured can be subtracted from the image area signal to remove the read noise from the data, this is shown in Equation 6.11 below (Janesick, 2007).

$$S(DN) = \sum_{i=1}^{N_{Plx}} \frac{S_i(DN)}{N_{Plx}} - S_{os}(DN) \quad 6.11$$

Where i is the current pixel, S is the signal level of pixel i in digital numbers, S_{os} is the average of the overscan signal level and N_{Plx} is the number of pixels in the frame of interest.

6.2.2 Shot Noise

Shot noise is related to the time when photons arrive on a detector surface and is a fundamental noise source associated with the nature of light (Janesick, 2007). The shot noise regime dictates that the average noise in a flat field image is equal to the square root of the signal level, shown in Equation 6.12 (Janesick, 2007), as determined by Poisson statistics. Shot noise is the only source of noise at the input of the detector and as such is not contributed to by the camera system. Thus it cannot be removed from the data. A gradient of $\frac{1}{2}$ represents the shot noise regime on the log-log PTC plot due to the relationship shown in Equation 6.12, an example of which is displayed in Figure 6.58.

$$\sigma_{shot} = \sqrt{S} \quad 6.12$$

6.2.3 Fixed Pattern Noise

Fixed Pattern Noise (FPN) is so called because it does not vary between images at the same input signal level and is generally reported to be the result of pixel-to-pixel sensitivity differences. As such, FPN is directly proportional to the input signal level and it has a gradient of 1 on the PTC (Figure 6.58). It is dominant at larger signal sizes. Fixed pattern noise may also include the effects of particulates present on the detector surface and any optical aberrations in the camera system optics, the fact that it remains the same across images means it can be easily removed from the data during processing, by subtracting two identical frames shown by Equation 6.13, a technique known as field subtraction (Janesick, 2007).

$$\sigma_s^2 = \sum_{i=1}^{N_{Pix}} \frac{[S1_i(DN) - S2_i(DN)]^2}{2 \times N_{Pix}} \quad 6.13$$

Where S1 and S2 are each of the identically illuminated flat field frames, N_{Pix} is the number of pixels in the frame, i is the current pixel number and σ_s^2 is the variance with FPN removed. A factor of two is included in the denominator because RMS noise increases by $\sqrt{2}$ in the resultant frame (Janesick, 2007).

6.2.4 Full Well Capacity

The final noise regime labelled in Figure 6.58 is the full well capacity, with its representative drop in measured noise. This characteristic is caused by charge spilling, or blooming, into adjacent pixels when they have reached saturation causing an averaging effect which reduces the variance in the measured signal.

The photon transfer curve, presented in Figure 6.58 is raw data extracted from the images captured using the CCD204 test camera and defining regions of interest as indicated in Figure 6.59. As the data are currently unprocessed, all the noise sources are still present and values of mean signal and standard deviation are given in units of digital numbers (DN) as determined by the analogue-to-digital converter in the camera output electronics. The following section describes how these data are obtained, and also how they are processed to calculate the camera gain factor (e-/ADU), which enables the conversion from digital numbers (i.e. the output from the camera system) to electrons. The following sections also show the results when the unwanted noise sources are removed from the data and the information is reduced to the shot-noise limited curve.

6.3 Obtaining the Photon Transfer Curve

The PTCs presented here are generated using an LED for illumination; the LED is mounted within a sealed vacuum chamber with the CCD, but is far enough away from the CCD to provide an approximately flat field. The LED is active for the duration of the integration period and the light intensity produced by the LED is fixed by the supply current, which is limited by a small resistor.

The mean signal level measured in the image is varied by changing the integration time, which is

the amount of time in which the CCD is acquiring an image. This method is used because it offers linear increase in signal size with increased integration time, as displayed in Figure 6.65, and also keeps the drive electronics and programming relatively simple.

The CCD204 used in this study was previously used for a proton irradiation study, as such there are areas of the device which have been exposed to high levels of radiation equivalent to the predicted end of life dose for the Euclid mission (Gow, et al., 2012). There are several defects and cosmetic blemishes visible in all the images captured using this CCD (Figure 6.59). The most obvious defect is in the bottom right hand corner, but there are also several bright columns and rows. This device does not meet the high optical specification demanded of a flight model, but is deemed adequate for scientific analysis and characterisation because it meets all other specifications.

It is important to remove the unnecessary noise sources present in Figure 6.58, as described in the previous section, for accurate analysis of the gain conversion factor and hence FWC. It is possible to process the data such that only the noise sources at the input of the detector (i.e. photon shot noise) are present in the measurements.

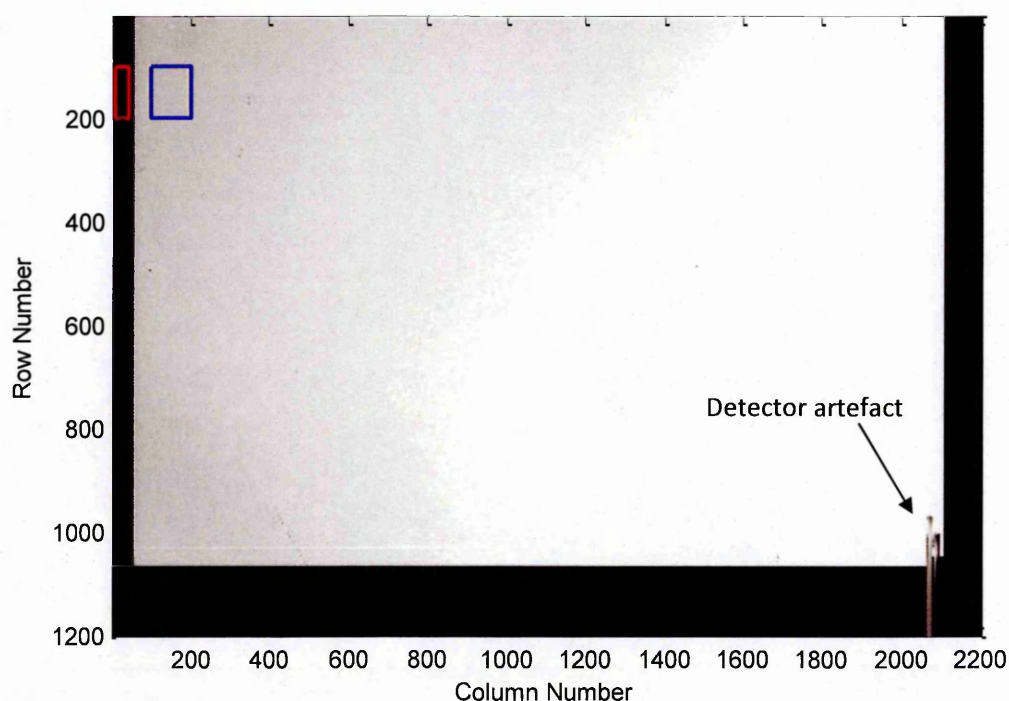


Figure 6.59: Flat field illumination on the CCD204 produced using an LED. The blue box is the region of interest (ROI) selected for PTC measurements. The ROI is small to reduce systematic errors, but large enough to include several hundred pixels for reliable measurements. The red box is the OS ROI used for read noise subtraction. Some defects are clearly visible in the image.

Figure 6.59 shows a flat field; these are unprocessed data and as such is made up of each of the noise sources that were shown in Figure 6.58. The defects in the CCD contribute to the fixed pattern noise visible in the PTC (Figure 6.58). The data presented in this chapter are from a 100x100 ROI shown in blue in Figure 6.59. The overscan area used to remove read noise during PTC processing will be located in the serial overscan, shown in red on Figure 6.59, and will usually correspond to the row numbers of the image area ROI because read noise may vary slightly from row to row.

6.3.1 Choosing The Region of Interest

The flat field provided by the LED is not ideal because the illumination level is non-uniform across the device. The non-uniformity is visible in Figure 6.59 as a slight gradient in the illumination level across the device, getting brighter in the lower right corner. The variation in illumination across the detector contributes to the variation recorded in the FPN section of the PTC, but this can

again be limited by introducing a smaller region of interest and even eliminated altogether through field subtraction, described in the next section. This is demonstrated in Figure 6.60 and Figure 6.61.

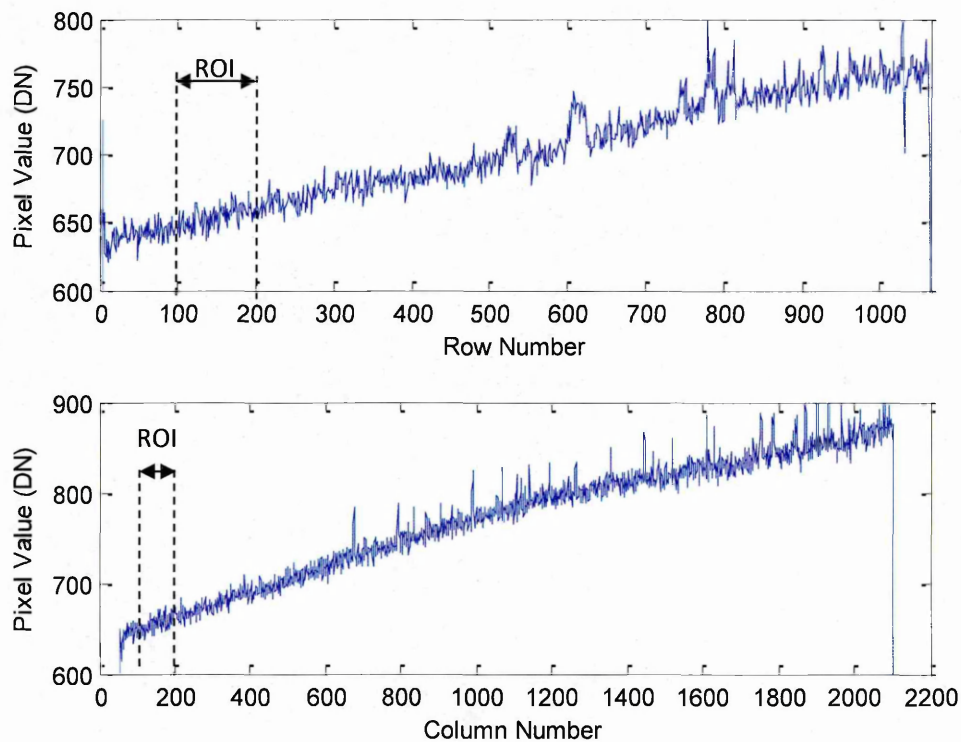


Figure 6.60: Variation in pixel signal level across the device for a flat field produced by the LED. Looking along column 150 (top) and along row 150 (bottom) which both pass through the chosen ROI, indicated. Rows towards the bottom and columns on the right collect more charge than other areas of the device because the illumination level is higher in these regions.

Figure 6.60 gives pixel value as a function of pixel number in both row and column directions to show the variance caused by the non-uniformity of the flat field in these particular rows and columns. The flat field varies between ~650-900 DN in the row direction, ignoring bright and dark defects. This is ~28% of the total signal level in this example, but the flat field varies depending on the row chosen and the signal level at which the measurement is taken. Similarly the flat field variation in the column direction is ~22% of the maximum signal level.

By choosing a small ROI, 100x100 pixels in the case of the PTCs presented in this chapter (located at pixels 100 – 200 in both row and column directions) the flat field variance is reduced to less than 3% of the total signal in the row direction and ~3% in the column direction, while retaining a sufficiently large number of, necessary for a good statistical analysis.

6.3.2 Field Subtraction

Field subtraction reduces the illumination non-uniformity to zero, whilst also eliminating the FPN caused by defects, although both effects are limited initially through the careful selection of the region of interest. A detailed description of the field subtraction method was given in Section 6.2.3. The effect of field subtraction can be seen in Figure 6.61, (i.e. the flat field gradient no longer exists) but the data now varies around a mean signal level of zero, so the signal level is lost. It should be noted that although the pixel-to-pixel variation appears to have increased in Figure 6.61, the scaling on the y-axis differs from that presented in Figure 6.60.

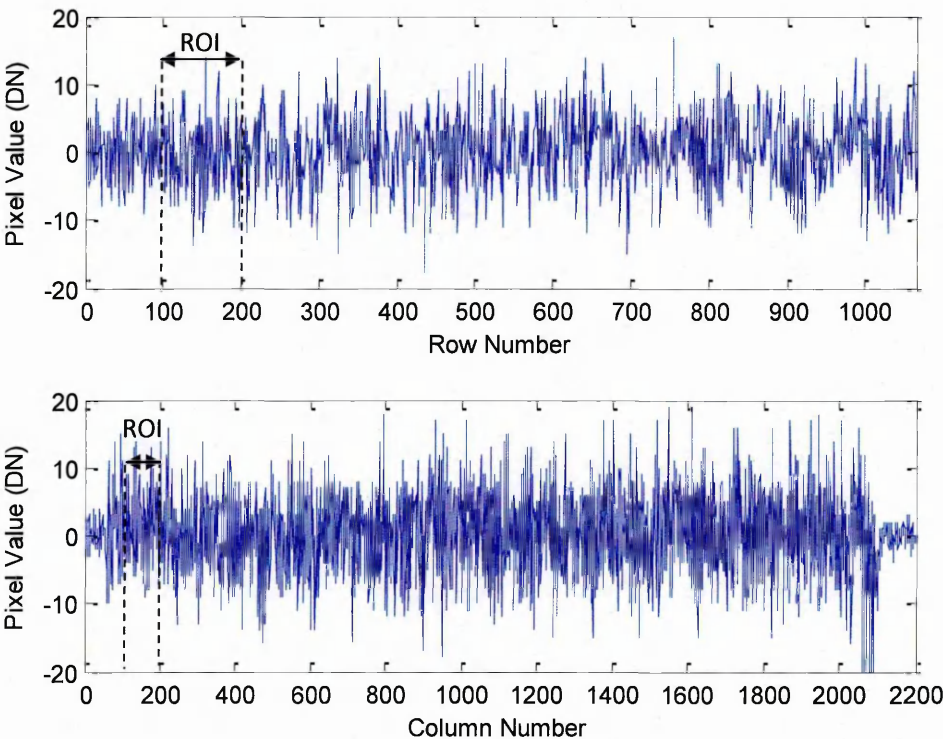


Figure 6.61: Field subtraction removes the illumination gradient seen in Figure 6.3 along with other sources of FPN, whilst maintaining the random variance associated with shot noise.

Field subtraction removes the extra variance associated with all FPN sources and the FPN regime of the PTC is reduced to an approximately shot noise limited data set at large signal. The new gradient approaches the shot noise slope of $\frac{1}{2}$ (Figure 6.62). In this example the read noise has also been removed using the over-scan subtraction technique, described in Section 6.2.1, producing a gradient of $\sim 1/2$ over the entire signal range. The standard deviation of the processed data is plotted against the mean signal level from the original data set to produce the “shot noise limited” photon transfer curve.

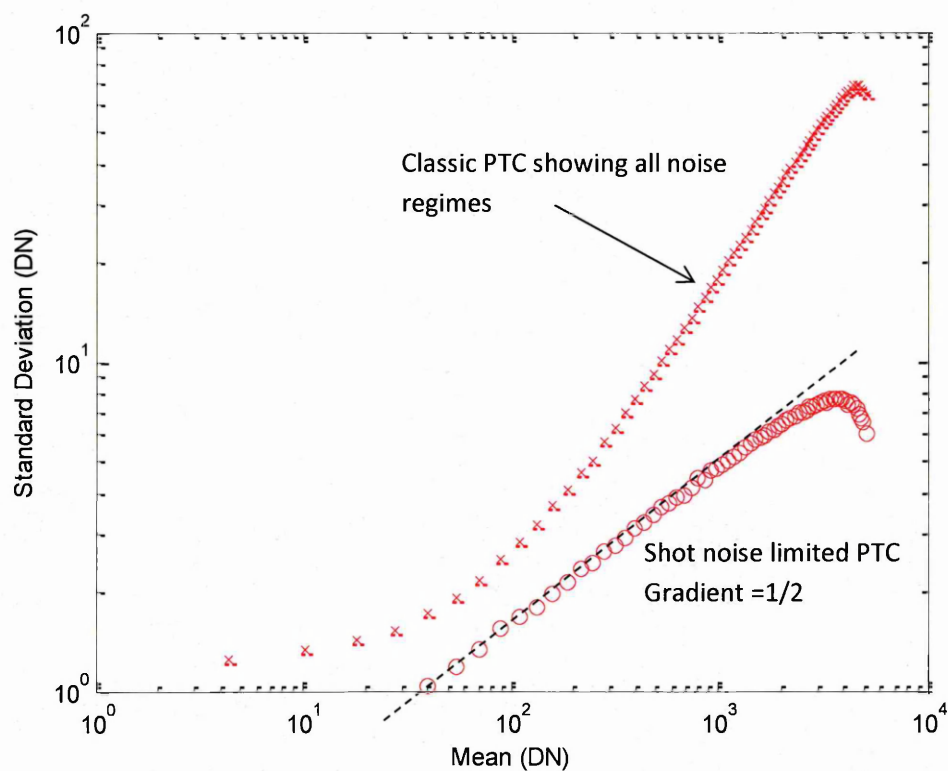


Figure 6.62: A classic PTC, as seen in Figure 6.58, plotted against a shot noise limited PTC with read noise and fixed pattern noise removed. The shot noise limited curve gives an accurate gain calibration for the camera system.

Calculating the total gain value for the camera system, K (e-/DN), gives the conversion factor for changing between units of digital numbers (DN), which are output from the analogue-to-digital converter in the camera system, and units of electrons. The camera gain can only be calculated once read noise and fixed pattern noise has been removed from the data set. Camera gain is

calculated from the PTC data by calculating the gradient of the signal variance versus mean signal plot, shown by Equation 6.14 and graphically later in Figure 6.64.

$$K \left(\frac{e^-}{DN} \right) = \frac{S(DN)}{\sigma_{shot}^2(DN)} \quad 6.14$$

The gain may also be found by manipulating Equation 6.14 to get:

$$\log K \left(\frac{e^-}{DN} \right) = \log S(DN) - 2 \log \sigma_{shot}(DN) \quad 6.15$$

Then, when $\sigma_{shot} = 1$, Equation 6.15 will reduce to:

$$K \left(\frac{e^-}{DN} \right) = S(DN) \quad 6.16$$

Equation 6.16 shows that the gain is equal to the signal level when $\sigma_{shot} = 1$ (Janesick, 2007), this corresponds to the point where the shot noise limited data crosses the x-axis on the log plot shown in Figure 6.62. The accuracy of the gain conversion value can be confirmed by converting the PTC data to units of electrons and re-plotting. If an accurate gain value, K , is used, the mean signal value should follow the square root of the standard deviation of the signal precisely, which is the shot noise relationship. The shot noise slope is marked as a dotted line on Figure 6.63 against the PTC data which has been converted to units of electrons. If a precise gain factor is not used, the data points will not lie on the dotted line in Figure 6.63.

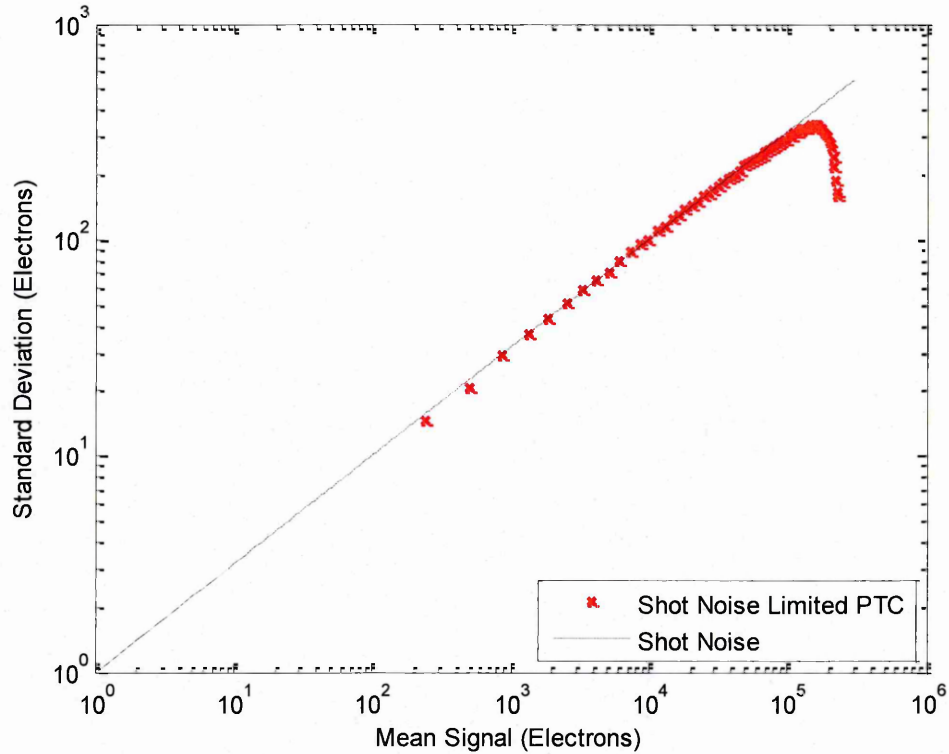


Figure 6.63: PTC with FPN and read noise removed. The data are converted to units of electrons using the gain calibration calculated from the shot noise limited slope of Figure 6.5. By plotting the data against the theoretical shot noise slope the accuracy of the system gain calibration can be evaluated (Janesick, 2007).

Once the conversion factor is confirmed and the PTC data are converted to units of electrons the value of FWC can be extracted from the data, where it is still characterised by a drop in the measured variance. By plotting the mean-variance data on a linear scale the FWC rollover can be extracted more easily (Figure 6.64). The linear plot of variance vs. signal should also make the non-linearity at high signal levels more obvious. Where the gradient should be 1 over the entire signal range to the FWC roll-over in Figure 6.64, but the data deviate from the expected Poisson distribution. This non-linearity has recently been associated with a small correlation (<1%) between the signal electrons in adjacent pixels during charge collection (Stefanov, 2014). This effect varies between detectors, but becomes more pronounced in thicker deep depletion devices, which tend to be manufactured on higher resistivity substrates.

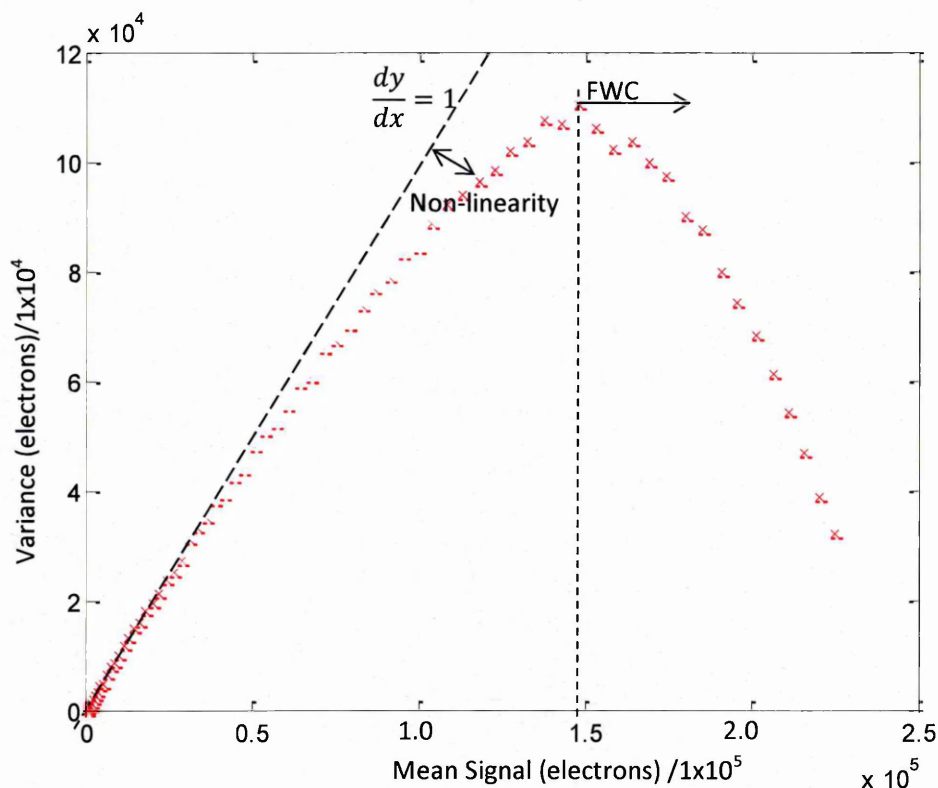


Figure 6.64: The shot noise limited photon transfer curve is re-plotted using Variance vs. Mean Signal to show the FWC rollover point more clearly. This plot also emphasises the deviation from linearity as the data should follow a gradient of one.

All values for FWC in the CCD204 tests presented are calculated using a data set similar to Figure 6.64. The FWC signal level is measured corresponding to the peak variation value before the rollover where the variance begins to reduce. In the case of Figure 6.64 this has been marked and corresponds to a FWC value of $\sim 1.5 \times 10^5$ e-.

6.4 Photon Transfer Method

The LED is held on at a constant intensity for the duration of the frame integration. To accumulate mean-variance data at a series of increasing signal sizes the length of integration time is increased and several frames at each signal size are recorded. The camera system used in this analysis has several LEDs mounted in the vacuum chamber giving the option of a range of wavelengths. Each LED is tested for its linearity over a range of integration times which is shown in Figure 6.65.

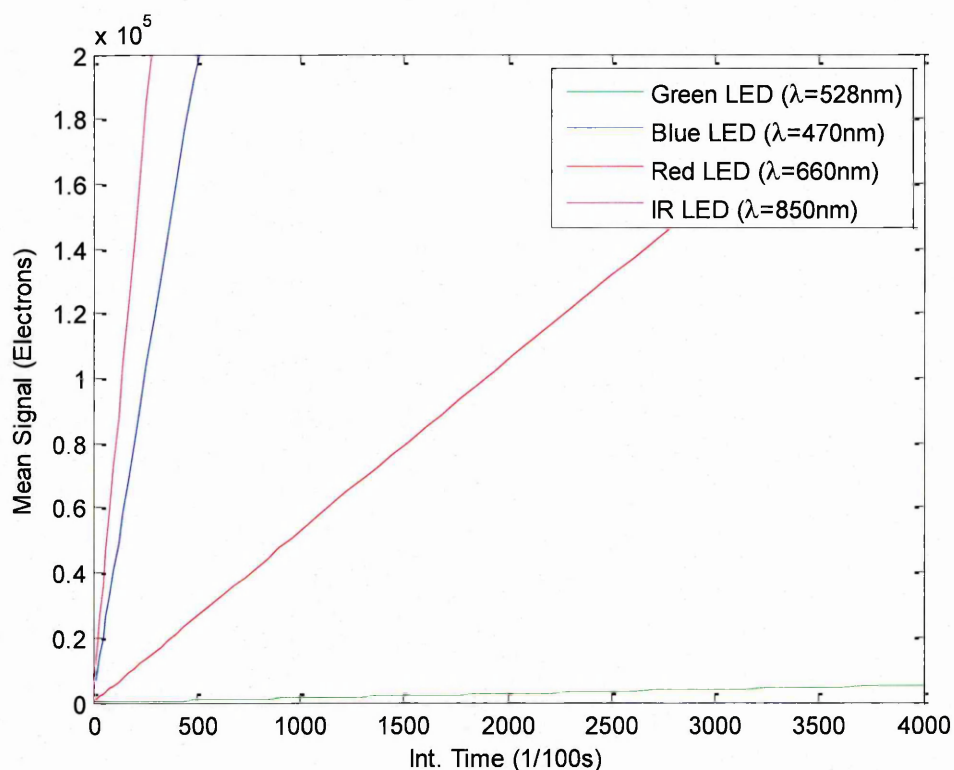


Figure 6.65: LED signal linearity as a function of integration time, for a number of different LED wavelengths ranging from the visible green, blue and red, to IR.

Figure 6.65 shows the increase in signal size over a range of frame integration times for each of the LEDs present in the vacuum chamber. FWC in the CCD204 image area is expected to be in the region of 190k e⁻. In this system the green LED can be eliminated immediately because it is not bright enough to produce a signal level comparable to FWC, the signal level does not surpass 10k e⁻ even after a 40s exposure. Blue and IR LEDs are very bright, as shown by the rapid increase in signal level over a short time period. The brightness of these LEDs can be reduced by introducing a series resistor, which would limit the current through the LED. Alternatively the red LED shows good linearity and reaches FW signal level within the maximum integration period, with no modifications to the system.

The red LED is chosen for the on-going data collection; all of the PTC data presented in this chapter will be produced using the red LED, unless stated in the text. The wavelength of the light used to produce the flat field should have no effect on the device FWC.

6.5 Device Operation

Full well capacity is a complex parameter. While the simplistic description of charge spilling from a full potential well into adjacent potential wells is accurate, it must be remembered that the potential field within a CCD is constantly changing during charge transfer to allow charge to be read out of the device. In some cases the limiting FWC may not be reached for the static field case, during image integration, but may still occur when charge begins to be shifted out. This effect will be dependent upon the readout sequence used to move the charge through the registers.

It is important to ensure that the conditions under which the FWC is measured in the CCD204 test camera match the conditions under which the devices are simulated for a reliable verification. This is especially important in light of the FIBSEM results which show some undersized gates, as these will limit FWC during readout. During normal operation the clock bias varies between two voltage values to collect charge and alternately readout the CCD. This section considers what effects the readout clocking sequences for the four-phase image area have on FWC, taking into account the varying gate widths which might be expected in the CCD204 image area as indicated by the FIBSEM analysis.

FWC is the maximum amount of charge that can be stored in a particular potential well, and is surpassed when charge begins to spill into adjacent pixels. The number of active phases during image integration will affect the FWC measured by determining the lateral extent of the potential well. Charge is integrated under two phases during the normal operation of the Euclid device.

FWC can also be limited if charge spills during the readout sequence, when it is transferred from pixel to pixel. The readout sequence determines the phases that are active during integration and the sequence in which the electrodes are clocked for readout. As some of the electrodes are suspected of being over-etched during manufacture, some of the gate widths may be undersized, while those adjacent to the undersized gates become oversized to fill the extra space available and compensate the over etch of the adjacent layer.

6.5.1 Sequencers Used for Data Collection

The sequencer determines the order in which phases are storing charge during image integration and readout. This section describes two different sequencers which were used to test the FWC of the CCD204 test device, the results of which are presented in later chapters.

With the four-phase image area of the CCD204 a minimum of two adjacent phases can always remain active during readout. Figure 6.66 shows a portion of the readout sequence used for the image area with a schematic representation of the clock waveforms. This is a 323 sequence, similar to the one which will be used in the Euclid mission. Charge moves from gates 1 and 2, to gates 1, 2 and 3 before being confined to gates 2 and 3. The bias on gate 4 is then increased so that charge is shared across gates 2, 3 and 4, before the bias is reduced on gate 2 confining charge to gates 3 and 4. This sequence repeats moving from two gates to three gates until charge is moved one full pixel. Using this readout sequence, the FWC should only be limited in the smallest pair of electrodes during readout.

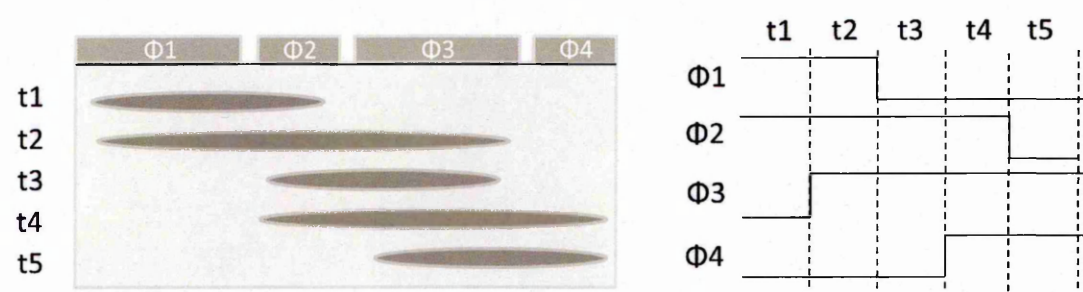


Figure 6.66: Schematic representation of the charge packet location within a single pixel cell for a representative section of one of the readout clocking schemes. The charge packet is always under a minimum of two active phases during readout, to avoid limiting FWC. This is known as a 323 readout sequence.

An alternative readout sequence has also been tested during the course of this work, under which charge is always confined to two phases during both integration and readout. This is a 222 readout sequence and is shown schematically in Figure 6.67. Charge moves from gates 1 and 2 to gates 2 and 3, with a small overlapping region in the waveforms as one phase is clocked low and another clocked high almost simultaneously. The 222 sequencer has an advantage of larger

barrier phases between charge packets presented by two unbiased electrodes, which may improve FWC by presenting a more effective barrier to charge spilling from well to well.

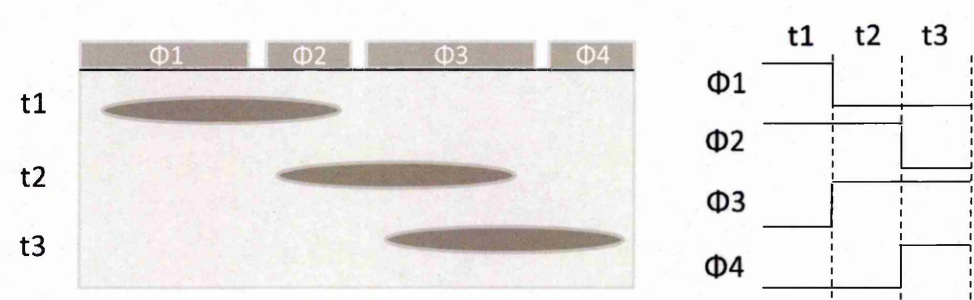


Figure 6.67: A section of the clocking scheme used for the 222 readout sequence, along with a schematic representation of charge packet locations during readout. Charge is never in a well larger or smaller than two active phases which should has the same advantage of the 323 sequence, whilst maintining larger barrier phases.

The serial register is a three phase structure, so the options for the readout sequence are more limited. The FIBSEM results for the CCD273 serial register show that the poly-silicon 1 layer is severely undersized, which will limit the FWC of the serial register. As the serial register is a three phase structure the readout is achieved using a 121 sequence, shown in Figure 6.68, which is representative of the device operation for the Euclid mission. In the event that the signal level reaches the register FWC, which is designed to be much larger than the image area FWC, the charge will tend to spill during the readout process when the charge is transferred into the register.

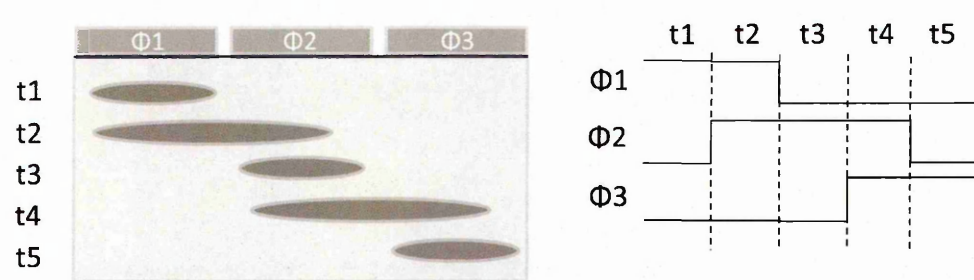


Figure 6.69: Charge packet location within a single register cell for a representative section of the readout clocking scheme, showing that the charge packet is confined alternately under one or two active phases during readout. This is known as a 121 readout sequence and is representative of the sequence which will be used during the Euclid mission.

In terms of the PTC measurements, charge spilling between pixels during integration, or during readout is indistinguishable. Both scenarios involve charge spilling into adjacent charge packets causing an averaging effect along a transfer channel. The tests carried out in this chapter use either the 222 or 232 readout sequence for the parallel registers in the image area, in combination with the standard 121 readout sequence for the serial readout register. Each measurement will have an associated description of the readout mechanism so they can be distinguished.

6.6 CCD Operating Voltage

The voltage applied to the gate electrode determines the extent of the depletion region into the substrate and the maximum potential formed in the buried channel. As such a higher gate bias causes a “deeper” potential well to form and the FWC of the structure scales with an increase in operating voltage. However, there is a limit to the FWC scaling because an increased gate bias brings the buried channel closer to the surface interface, increasing the probability of charge interacting with the interface states. Where surface interaction occurs, electrons will become trapped by interface states reducing CTE and reducing the variance of the PTC, similar to the effect seen when charge blooms across pixels. This condition is termed the “surface FWC” and causes the FWC that previously increased with operating voltage to drop with further voltage increases, as measured by the PTC.

PTCs are generated over a range of operating voltages and the results are displayed in Figure 6.70. The measurements in Figure 6.70 are taken while integrating under two phases with the 232 readout sequence, which is employed because it reflects the mission operating parameters. Figure 6.70 shows the increase in FWC depending on operating voltage, but as this figure is densely populated the relevant FWC values are extracted and plotted in Figure 6.71, alongside the same values recorded under the same conditions, but while using the 222 readout sequence.

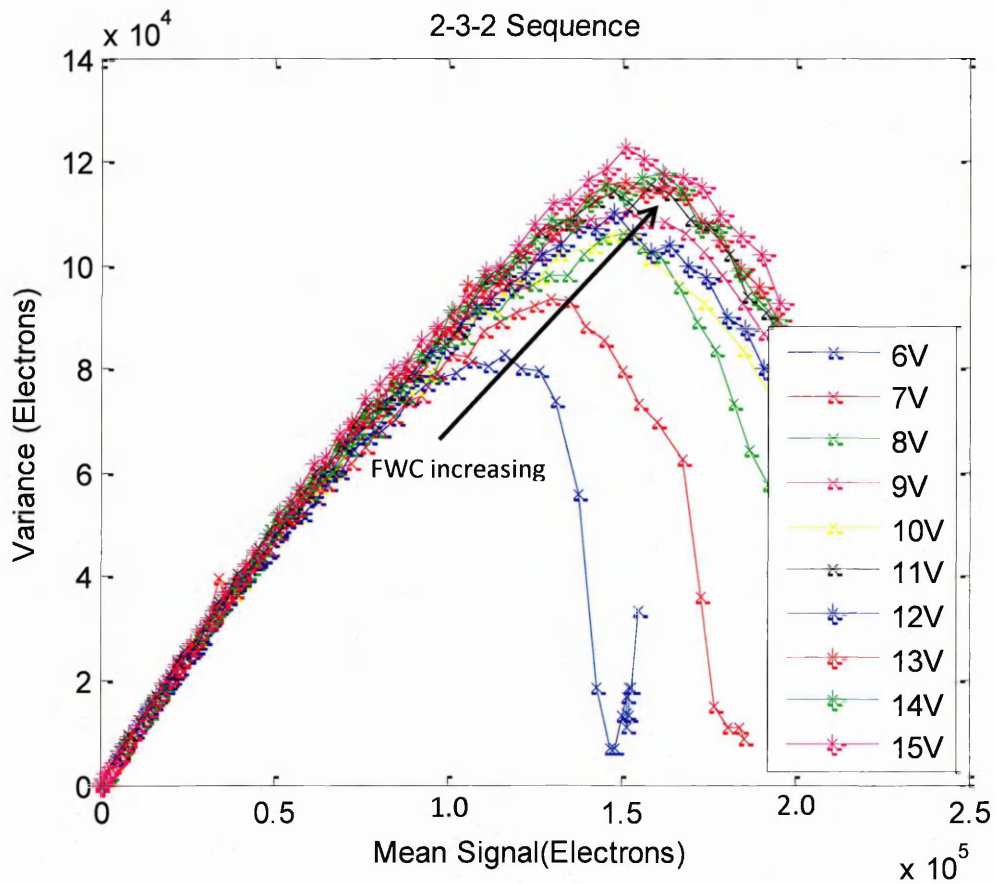


Figure 6.70: PTCs measured at different operating voltages while integrating under two phases using a 232 readout sequence, showing the increase in FWC as operating voltage increases.

Figure 6.71 shows that the FWC is not simply dependent on operating voltage and device architecture, but also varies according to the way the device readout is operated evident due to the variation in values when different sequencers are used for readout. These factors will need to be taken into consideration when comparing the FWCs extracted from the models. Additionally Figure 6.70 shows the non-linearity noted in Figure 6.64 becomes less severe at higher operating voltages.

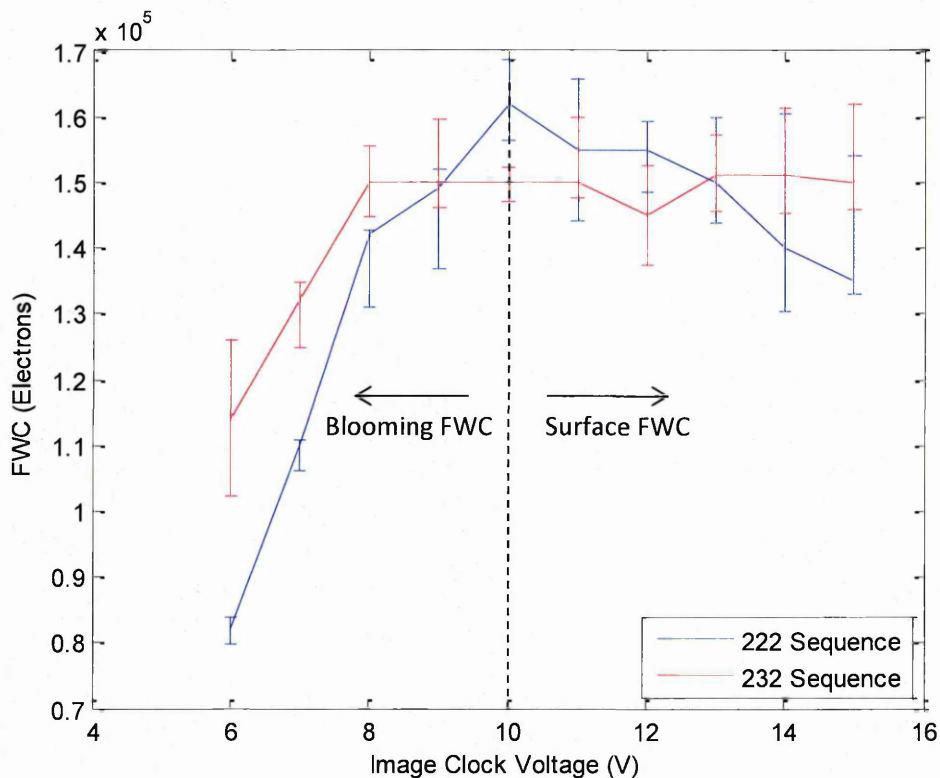


Figure 6.71: FWC measured from PTCs at different operating voltages for two different readout sequences. The 2-2-2 readout sequence shows the characteristic drop at higher voltages expected from surface interaction and indicates a channel potential of 10 V.

Figure 6.71 shows the FWC results over the same range of voltages for both a 222 readout sequence and a 232 readout sequence. The 222 readout sequence displays the expected peak (at 10 V) and subsequent drop in FWC due to surface interaction at higher voltages. This FWC distribution indicates the optimum operating voltage and also the channel parameter of the device, which is at the expected value of 10V.

The FWC data in Figure 6.71 shows that there is a plateau in the FWC above approximately 8-9 V when using the 232 readout sequence. The expected drop in FWC due to surface interaction does not occur, which indicates that charge is continuing to bloom across pixels even at high operating voltages. As the 232 readout sequence involves using a single phase as a barrier at some stages of the readout sequence, the plateau in Figure 6.71 is probably due to an inadequate barrier potential when a single phase is used as a barrier. As an over etch problem has already been demonstrated in these devices it is likely that one of the over-etched poly-silicon layers is

responsible causing an unexpectedly small gate in one of the poly-silicon layers. The reduction in the potential barrier presented by the undersized gates may be exaggerated by the fringing fields from the active gates on either side of the barrier phase.

Figure 6.71 indicates the optimum operating voltage for the device and this varies depending on the readout sequence used. Maximum FWC is desirable, but without the contact at the surface interface, which occurs at higher voltages, as this will impact charge transfer efficiency. Figure 6.71 shows the optimum operating voltage is 8 V when a 232 readout sequence is used, while a 222 readout sequence should operate with a clock high voltage of 10 V.

When the 222 sequence is used the barrier between charge packets is a minimum of two electrodes wide at all times during the readout sequence. While the 232 sequence results in a potential barrier that varies between one and two electrodes wide. The reduced barrier in some stages of the 232 sequence is the most likely cause of the difference in FWC values achieved between these two sequencers. The FWC values present in Figure 6.71 can be compared against the values extracted from the Silvaco models, under some of the same operating voltages (Table 6.3 and Figure 6.72). The method of determining FWC in the device models has been described in Chapter 4.

Voltage (V)	Modelled FWC (k Electrons)	Measured FWC (Electrons)	
		2-2-2 Sequence	2-3-2 Sequence
6	160 (+/-10k)	82k (+/-2k)	114k (+/-10k)
7	169 (+/-10k)	110k (+/-3k)	132k (+/-5k)
8	173 (+/-10k)	142k (+/-10k)	150k (+/-5k)
9	169 (+/-10k)	149k (+/-10k)	150k (+/-6k)
10	170 (+/-10k)	162k (+/-8k)	150k (+/-2k)
11	175 (+/-10k)	155k (+/-9k)	150k (+/-5k)
12	Not modelled	155k (+/-5k)	145k (+/-6k)
13	Not modelled	150k (+/-7k)	151k (+/-6k)
14	Not modelled	140k (+/-15k)	151k (+/-6k)
15	Not modelled	135k (+/-10k)	150k (+/-6k)

Table 6.3: List of the FWC values measured and modelled for a range of voltage levels. These include the FWC values for two different sequencers used on the CCD204. The errors associated with the FWC values indicate the uncertainty on the exact location where the roll-over occurs.

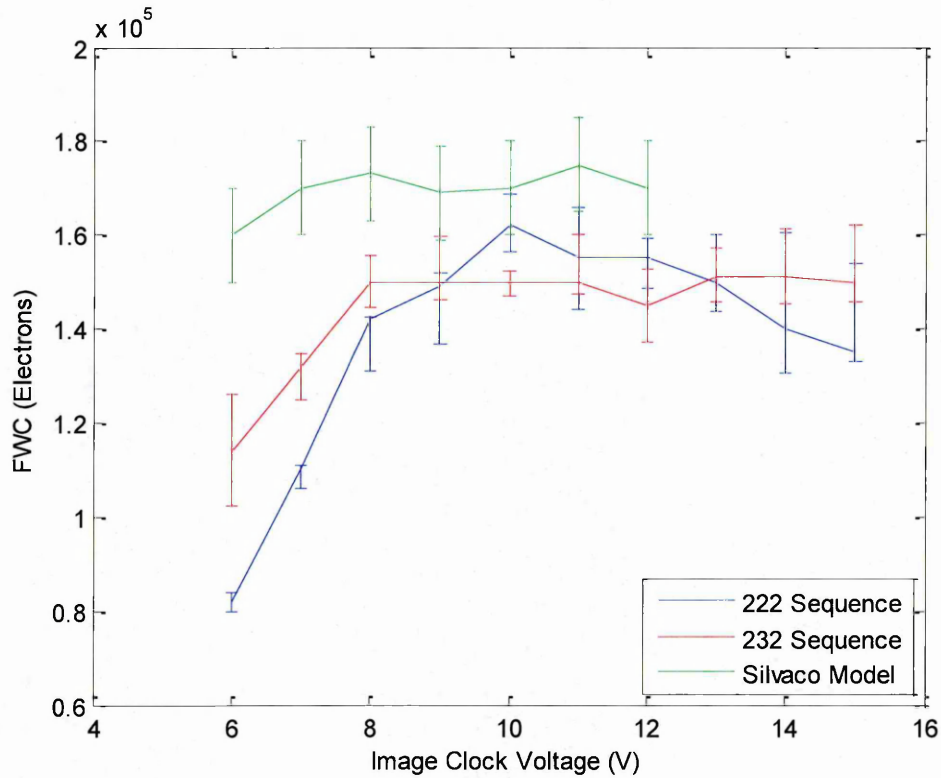


Figure 6.72: The modelled FWC plotted against the measured values. The modelled FWC overestimates the FWC, which may be attributed to the models taking no account of the manufacturing variation observed in the FIBSEM analysis.

Figure 6.72 shows that a large variation is possible in the FWC measurement from the same test device depending on the way the device is operated. The device simulations are single cell structures and the values obtained are measured by direct probes within the models, so no readout method is used to obtain measurements which may be the cause of the overestimate of FWC in the models. Also the following section describes a variation from design in gate deposition widths shown through FIBSEM image analysis, meaning that the models may define the gate electrodes to be larger than they are in the test device, which would affect FWC.

6.7 FIBSEM Investigation

The FWC values extracted from the device models are consistently overestimating the values measured in the test device. These results motivated an investigation to measure the gate dimensions in an actual device to confirm that they have been manufactured to the design. A reject CCD273 wafer became available during the course of this work representing a good

opportunity to examine directly the physical gate structure in a Euclid CCD. The focused ion beam scanning electron microscope (FIBSEM) is an instrument that allows precision etching of targeted structures using a focussed ion beam. The FIBSEM then enables cross-sectional images of those structures to be captured using the scanning electron microscope. This investigation was completed using the FIBSEM at The Open University with help from the FIBSEM operator Dianne Johnson and Neil Murray.

The parallel register of the Euclid CCD is a four-phase structure, which is manufactured using two-level poly-silicon gate processing (Figure 6.73) where only one gate overlaps the gates adjacent to it on both sides. It is possible to define the poly-silicon layers from this image, where the flat gates were deposited first are generally phases 1 and 3, and the gates with overlaps were deposited afterwards, phases 2 and 4.

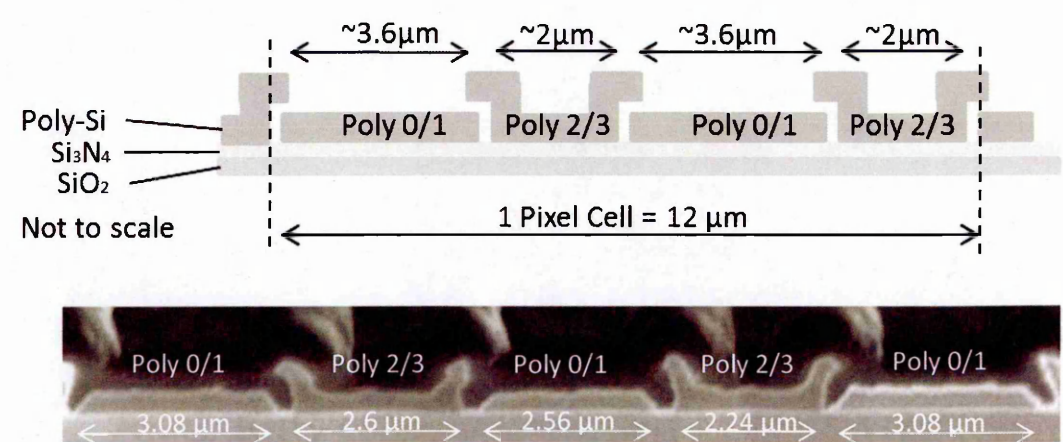


Figure 6.73: FIBSEM image of the parallel register electrodes in a reject CCD273 compared against a schematic representation of the expected layout and dimensions, with inter-electrode gaps of 0.25 μm. These gates are located close to the charge injection structure in the centre of the device.

Summing the measured gate widths of the four phases here, along with the inter-electrode gaps of ~0.25 μm gives a total pixel pitch of 11.73 μm which is ~0.25 μm smaller than the design pitch of 12 μm. The inter-electrode gap has a nominal width of 0.25 μm, although there is a slight variation in the thickness between some gates. The dielectric layer between the gates and the

substrate is visible in these figures as a white line because it is too narrow to be resolved with good definition.

As specified in the design criteria, every second gate in the image area should have the same gate width, nominally $2\mu\text{m}$ and $4\mu\text{m}$. One of each of the four phases which define the Euclid pixel are displayed in Figure 6.73. It is interesting to note that the width of the fifth gate matches the first gate width exactly and as it is the largest gate in the image, therefore it is assumed to be one of the larger designed gate widths which should be $3.5\mu\text{m}$ - $4\mu\text{m}$, though here it is smaller than expected. It is also expected that the centre gate would also match this measurement – but it is undersized by $\sim 0.5\mu\text{m}$ from the already undersized gates. The overlaps seen in these images do not actually overlap the adjacent electrodes in any of the images, indicating that there is an over-etch in the manufacturing process after the poly-silicon layers are deposited, which would also explain the gate width deviation from design.

The register structure was also imaged using the FIBSEM, where the register is three-phase, with the fourth phase acting as a dump gate to a drain at the bottom of the register (not shown in Figure 6.74). The register was designed and initially modelled with equal gate widths, but Figure 6.74 shows that each phase is actually different size in this device. Charge is stored and transferred in this register between single phases, so the maximum FWC which can be measured in the serial register will be determined by the smallest gate electrode, in this case poly-silicon 1, which is $2.3\mu\text{m}$ wide. Modifications to the model may be needed to reflect the deviation from design, if the calculated FWC does not match that measured in the test device.

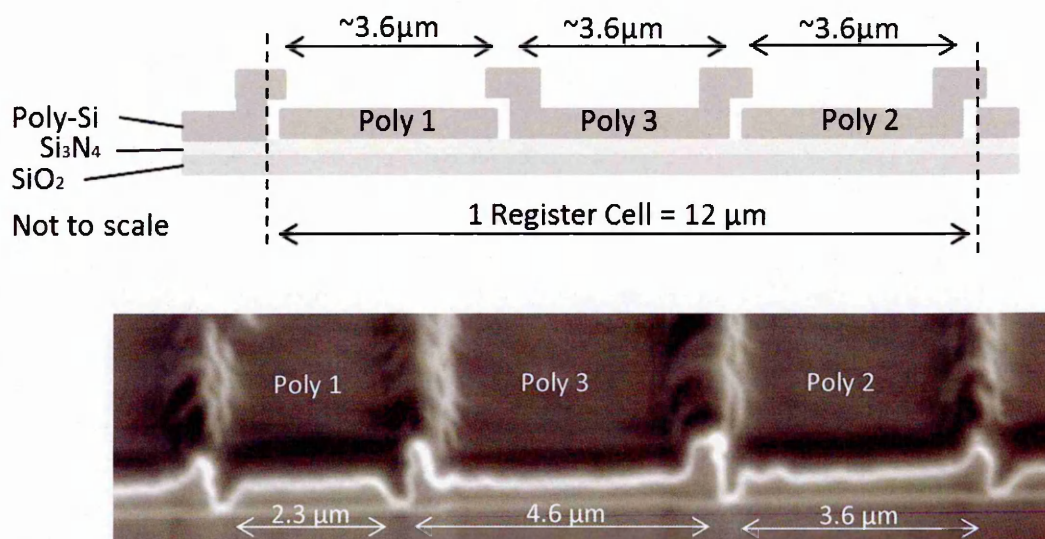


Figure 6.74: FIBSEM image of the serial readout register electrodes in the reject CCD273 wafer. These gates should all be manufactured to the same width, but they are different sizes.

The variations in gate geometry deviate from design, but do not prevent device operation. The Euclid test devices, and others manufactured under the same processes, perform well in experiments designed for characterisation and to test radiation damage effects (Gow, et al., 2012). Under normal operation the Euclid device integrates under two adjacent active phases in the image area, in this case the active area will not see any significant effects due to the compensating poly-silicon deposited adjacent to the over-etched layers (i.e. the oversized smaller gates). However, the total active area is still undersized by some margin, which will affect the charge packet dimensions and the FWC measured. This work helps to explain the difference between FWC in the models and that measured in the test device.

The test device used in this chapter for model verification is a CCD204. The images presented in this section come from a different device, the CCD273. The two devices were manufactured in a different batch several years apart, but their basic manufacture should be the same due to the similarities in device geometry and design. Caution is taken when attempting to compare the two.

The rest of this chapter is aimed at the development of modified device models which reflect the electrode layout measured in the FIBSEM images. These may improve the accuracy of the FWC calculated from the models, but it is not possible to calculate the actual electrode dimensions for

the test device used, because capturing cross sectional images using the FIBSEM destroys any device which is being imaged.

6.8 FWC with Single Phase Charge Collection

The FWC calculated from the models for different operating voltages consistently yielded results that overestimated FWC compared to the measurements from the CCD204 test device. It was suspected that the modelled gate dimensions were much larger than those which were present in the test devices, indicated by the FIBSEM measurements made on a CCD273. In this section the integration sequence is altered to allow integration under single phases. A PTC is generated while each individual image phase is used for image integration, so that FWC can be measured for each of the four phases separately. During these tests the readout sequence remains the same, with a 232 readout sequence in the parallel registers and the standard 121 sequence in the serial register. Using this readout sequence should ensure that charge collected by a single phase will not spill during the readout sequence.

These measurements will act to validate that the same over-etch problems revealed by the FIBSEM images for the CCD273, are shared in the CCD204, as the two devices share the same manufacturing processes. If the same problems discovered in the FIBSEM images of the CCD273 are present in this test device a number of different FWCs would be expected. However, if the gate widths follow the design criteria two separate FWCs should be measureable. Figure 6.75 shows that a number of FWCs are measured depending on which of the electrodes are active.

The labels used in Figure 6.75 to delineate each of the four image phases are those which are used in the software sequencer, so they bear no relation to the actual poly-silicon layer, as described during the FIBSEM analysis (Figure 6.73). With the information gathered so far it is not possible to discern which poly-layer is which in the test device. It is also not possible to determine what the poly-silicon dimensions are in the test device, but the dimensions used in the device models are modified to resemble the FIBSEM measurements performed on the CCD273 wafer in an effort to provide a better match to the modelled FWC with the FWCs measured in Figure 6.72.

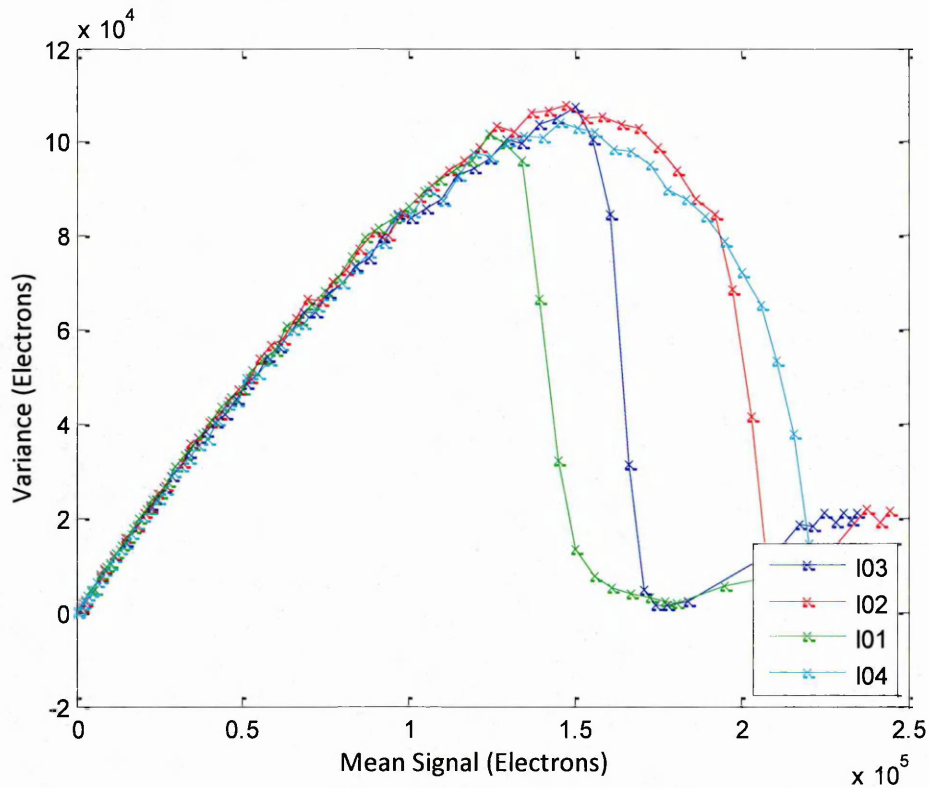


Figure 6.75: Shows the PTC generated for each of the four gate phases (I01 – I04), three different FWCs are visible. This indicates there are three different gate sizes, not two as designed.

The FWC can be extracted from the PTC under each image phase of the test device and the values differ, offering three separate FWC values. Two of the image phases provide the same FWC measurement, which is the largest FWC value measured, indicating two larger gates with the same dimensions within the pixel architecture. This FWC is $\sim 1.5 \times 10^5 \text{ e}^-$, which is measured under image phases I02 and I03. I02 and I03 will be adjacent electrodes in the parallel registers, indicating that the expected layout, which should alternate from large to small electrode dimensions, is not present in this device. The remaining image phases show two different FWCs, indicating that they are different sizes, these are measured at $\sim 1.25 \times 10^5 \text{ e}^-$ for I01 and $1.45 \times 10^5 \text{ e}^-$ for I04.

The FWC is modelled based on the designed dimensions 2 and 3.5 μm , along with simulations of devices with the same electrode dimensions measured in the FIBSEM images from the CCD273 wafer, which are 3.08, 2.6, 2.56 and 2.24 μm . Unfortunately a direct comparison between the

models and the measurements is not possible because it is not possible to measure the gate widths in the test device, but the results from both design and the FIBSEM dimensions are presented together in Table 6.4.

Gate Width (μm)	Method	Modelled FWC (Electrons)
3.5	Design	~168k (+/-10k)
2	Design	~100k (+/-10k)
3.08	FIBSEM	~142k (+/-10k)
2.6	FIBSEM	~130k (+/-10k)
2.56	FIBSEM	~126k (+/-10k)
2.24	FIBSEM	~105k (+/-10k)

Table 6.4: Lists the FWC modelled for the designed gate widths, where the dimensions are extracted from CAD drawing used for manufacture, and the FWC modelled for each of the gate dimensions measured in the FIBSEM analysis.

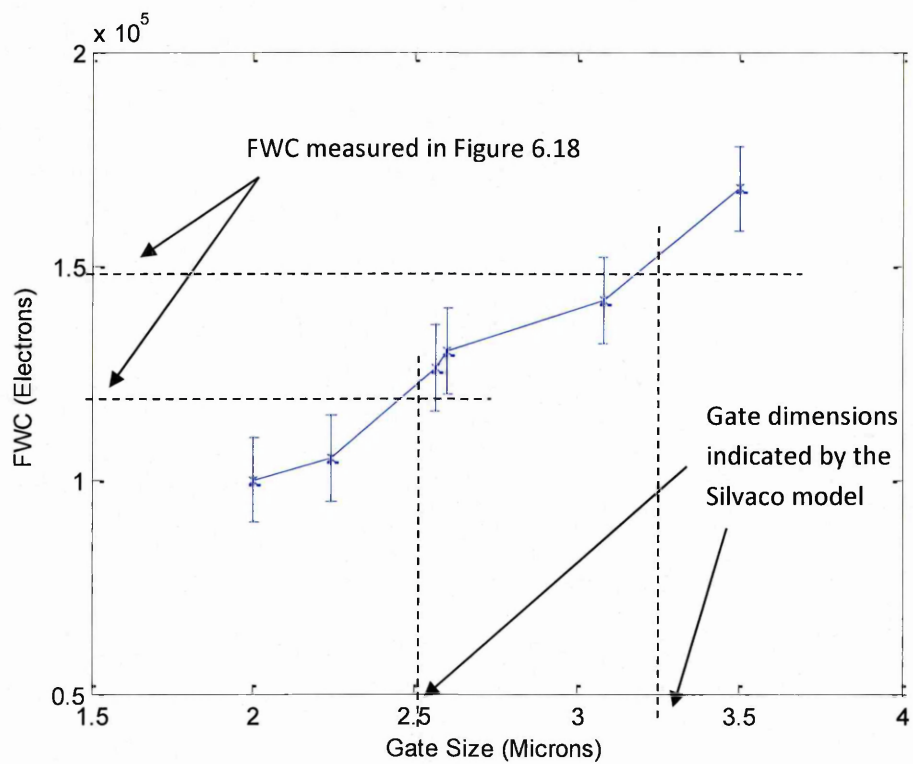


Figure 6.76: Plot of the modelled FWC for six different gate sizes, from Table 6.4, including the original models, based on CAD measurements, and gates modelled based on measurements extracted from the FIBSEM images. There are some slight deviations from the linear trend and error bars due to the way that FWC is modelled, which is described in Chapter 4. The dashed lines mark the gate dimensions which tie in with the FWC measured in Figure 6.75.

A comparison between the values from Table 6.4, and Figure 6.75, with the FWC which can be measured in Figure 6.75 shows a reasonable agreement between the values extracted from the models and the FWC measured under single phases in the test device. The FWC varies between $1.2 \times 10^5 \text{ e}^-$, $1.45 \times 10^5 \text{ e}^-$ and $1.5 \times 10^5 \text{ e}^-$ in Figure 6.75, agreeing with gate dimensions of approximately 2.45, 3.1 and 3.2 μm extrapolated from the model results in Figure 6.76. Taking these gate dimensions to be the assumed gate sizes that produced the results in Figure 6.75, the total pixel pitch would come to 11.95 μm , not including inter-electrode gaps, which ties in with the test device's 12 μm pixel size.

The FWC tends to be highly dependent on electrode dimensions and as such makes robust model verification difficult, due to the uncertainty in determining gate deposition widths within the specific test device on which measurements were carried out. Unfortunately it is not possible to confirm the exact electrode dimensions of the test device without destructive testing.

6.9 Implications for Euclid

The FIBSEM investigation was performed during the development stages of the Euclid CCD production. This work enabled e2v to modify the manufacturing process, so that the undersized electrodes present in these early evaluation devices should not be an issue for future test or flight models. This work is planned to be repeated on devices produced on the modified manufacturing process to ensure that the problems have been rectified, although none are yet available for testing.

Even so, the devices which are affected by the undersized electrodes do still pass the strict quality control and device characterisation of the Euclid project, and this would have a minimal impact on the mission performance. It was only when the more in-depth tests for model verification in this thesis were performed that these issues came to light.

6.10 Conclusions

FWC is a device parameter which is highly sensitive to a number of factors. Some of these are variables that are fixed at the time of manufacture, such as pixel architecture and doping, but many are operating parameters, such as the operating voltage or the readout sequence which can

be optimised during device characterisation. A number of the factors which may affect FWC have been explored in this chapter in an effort to verify device models simulating FWC using Silvaco TCAD. The first set of results, measuring FWC over range of operating voltages, showed the simulated FWC consistently to overestimate the parameter, when compared against the measurement values. These overestimates were assumed to be caused by the suspected over-etch observed in the electrode structures of a similar device. These might equally have been caused by some unforeseen effect of the dynamic potential field during readout, as the FWC models produced in Silvaco are based on the FWC of the static collecting field.

Tests exploring the operating voltage highlighted the effect that different readout sequences can have on the FWC measured in the test device. Two sequences were tested, the first resembling the planned readout sequence for the Euclid mission. This was a 323 readout sequence, possible because the image area is a four phase design leaving a minimum of one electrode to act as a barrier during transfer. The second sequence tested was a 222 sequence which produced much improved measurements and indicated a channel parameter and an optimum operating voltage of 10 V. The fact that the FWC varies depending on the sequencer used for readout makes model verification difficult.

In an attempt to tie measurements and models together, further tests were conducted by modifying the software readout sequence to capture images using only a single image phase. This test was repeated for each of the of the four image phases to note any changes between the FWC. If the test device followed the design criteria two distinct FWCs should have been measurable across the four phases. However, three separate FWCs were measured indicating that the device electrodes do not follow the design dimensions. This was confirmed during a study of the device electrodes where cross –sectional images of the electrode structure were captured using FIBSEM analysis. By modifying the device models, so that the electrode dimensions match those observed from the FIBSEM study, the modelled FWC provides a much closer agreement to measured values. The models have been used to extrapolate gate dimensions for the test device.

Although these cannot be directly confirmed, the total pixel pitch determined by the extrapolated gate dimensions agrees with the design dimensions.

6.11 Chapter Summary

This chapter introduced the PTC with a detailed description of the technique along with an analysis of the common measurements. The PTC is used here to measure FWC in a test device for comparison against device models. FWC has been shown to be dependent on a number of variables, some of which are fixed at manufacture such as the dimensions of the electrode architecture, and others which can be manipulated to find optimum operating conditions. FWC can be variable within the same device depending on the operating voltage producing larger or smaller potential wells, and also depending on the readout sequence used.

In light of the FIBSEM analysis, gate widths within devices are uncertain, and may be undersized causing deviations from the expected FWC and the Silvaco models. This makes accurate modelling and model verification difficult and causes some values to be consistently overestimated. Re-modelling based on the dimensions observed in the FIBSEM analysis of a CCD273 wafer improved model results, introducing a method for predicting the gate dimensions of the test device, by measuring FWC of individual electrodes and comparing against models of the devices. As the results shown here have a strong correlation with the device models, this also improves confidence in the accuracy of the models produced in Silvaco.

Chapter 7: EPER measurements

Extended Pixel Edge Response (EPER) is a technique commonly used to gauge an estimated CTE measurement for a CCD. In many cases the measurement can be made from a single flat field image. This chapter details EPER measurements made on a Euclid test device which were completed in an attempt to tie the charge packet modelling work presented in Chapter 5 to CTE measurements from a Euclid device.

7.1 Charge Transfer Efficiency

Charge Transfer Efficiency (CTE) is an important device parameter because it determines the percentage of charge that can be successfully transferred between pixels during the readout process. An efficient transfer is important because the number of pixels a charge packet must move through when it is read out of a CCD. Array sizes are variable, but can number in the millions of pixels in modern CCDs, meaning a charge packet will undergo thousands of transfers before it is output from the CCD. In such circumstances even a very small inefficiency will accumulate over the readout sequence and result in unacceptable charge loss from images. In some cases small portions of the charge packets may become delayed causing the charge to spread along the register and causing “charge tails” in captured images, which might be corrected as discussed in Chapter 5. In other instances the delay is so long that the delayed charge is not read out, and is therefore lost from the image altogether reducing the signal level.

This chapter explores Charge Transfer Efficiency (CTE) measurements made on a CCD273 test device with the aim of linking charge distribution models from Chapter 5. The main interest centres around the change in CTE with signal size, which is believed to be related to the charge distribution in the detector as it is transferred through the register channels. The Extended Pixel Edge Response (EPER) technique is used throughout this chapter because it offers a relatively simple method for collecting data over a range of signal sizes quickly, with no need for specialist equipment. The EPER technique cannot calculate absolute signal losses, but tends to give an estimate of CTE relative to signal size based on delayed charge transfer.

In buried channel CCDs, charge is held away from the Si-SiO₂ interface, so that it doesn't encounter surface traps, which impede the transfer process. However, bulk traps are still present in the buried channel, in much smaller concentrations, and act to reduce the CTE in buried channel devices in the same way but to a much lesser degree (Janesick, 2007).

Charge packets located close to the output amplifier will undergo relatively few transfers before output, when compared to a charge packet located in the uppermost corner of the imaging array, furthest from the output node. CTE is the same in both cases, but the overall charge loss will differ due to the number of transfers involved. Temperature affects the time constants of the trap capture and emission parameters as described by Shockley Read Hall theory in Chapter 2 (Shockley & Read, 1952). As the concentration of traps increases, a consequence of radiation damage (Hopkinson, et al., 1996) (Pickel, et al., 2003), the number of interactions between the charge packet and traps will increase causing a degradation in CTE. Similarly, where the trap concentration remains constant but the signal size increases, the charge packet will occupy a larger volume and interact with more traps, further degrading CTE (Hardy, et al., 1998) (Waczynski, et al., 2001).

Charge loss is an important factor when considering the CCDs that will be used for the Euclid mission, where the signal levels of interest will be of the order of 100s of electrons for the dimmest (most distant) objects. The aims of the Euclid mission make it important to produce methods that can mitigate or remove CTI effects from images. In many cases charge loss is not absolute, meaning that the charge lost from one charge packet will be re-emitted from the capturing trap into one of the following charge packets, as the transfer process progresses through the register.

Trap theory can be simplified by taking account of "slow" or "fast" traps. A fast trap will re-emit charge soon after capture, releasing charge back into its originating charge packet, with no net effect on the resulting images. Slower traps will emit into trailing charge packets, causing charge

tails or smearing images. Traps that are slower still will emit charge much later, after an image has been read out, resulting in signal loss.

Charge transfer efficiency (CTE) measurements are an important part of CCD characterisation that must be performed to predict device performance in harsh radiation environments (Gow, et al., 2012). CTE investigations generally centre around an investigation into radiation damage effects in CCDs to provide detailed and critical evaluation of device performance in hostile environments, such as those experienced in space (Gow, et al., 2012).

This chapter centres around CTE measurements made using the EPER technique that estimates CTE based on deferred charge in the overscan elements of a flat field image. The chapter will continue with a review of the similarities and differences between CTE measurements and the results from the charge packet models which have been presented in previous chapters.

7.1.2 Extended Pixel Edge Response

Extended Pixel Edge Response, EPER, measurements give an indirect indication of device CTE, through the analysis of deferred charge tails in the overscan regions of standard flat field images. The flat field measurements allow the illumination level to be easily varied through longer integration periods as in the mean-variance analysis from Chapter 6, giving a simple method for producing CTI measurements over a large signal range. The EPER technique cannot detect long time period losses from the charge packets, only those traps with time periods comparable to the frame capture and readout time, so it is only used to estimate a relative value for CTE. However, the measurements are useful for determining general trapping information and relative CTI in CCDs across a large signal range in a short period of time.

The flat field illuminations should result in a similarly sized charge packets in each pixel of the CCD array. Charge packets at the same signal level will have very similar volume and density characteristics, with small differences caused by any manufacturing variation from pixel to pixel and the Poisson distribution of photons incident on the pixels of the image array as discussed in Chapter 6. As the flat field charge packets are transferred through the array, each pixel should

have similar volume and density characteristics, therefore interaction with the same traps will occur repeatedly during image integration and readout (Waczynski, et al., 2001).

As each charge packet will occupy a similar volume in each pixel, the interacting traps will reach a steady state of occupancy (Waczynski, et al., 2001), owing to repeated interaction with almost identical charge packets. In more specific terms, traps that emit their captured charge within the frame readout time will recapture charge from the current charge packet in the pixel, because the same conditions that caused the original capture to occur will still exist. The same capture event will reoccur until all of the flat field pixels have been read-out, allowing traps to emit their captured charge into the trailing overscan pixels, which hold no signal charge, making re-capture unlikely.

With the entire image already read out of the device, the charge transfer process continues, but no charge is transferred. Traps which were previously at a steady state of occupancy will begin to emit charge into the empty potential wells of the overscan pixels as the charge packets move through the image array, therefore the voltage sampled at the output quantises only the reference voltage of the output node with system noise and the charge that has been delayed through trap interaction.

The deferred charge alters the signal level in the first few overscan pixels and is used to calculate CTI through the application of Equation 7.17 (Janesick, 2007). The quantity of deferred charge that is present in the overscan region is related to the number of interacting traps in the particular row or column being observed, while the number of interacting traps should be related to both the volume and density that the charge packets occupy versus the distribution of traps.

The variables used in Equation 7.17 are S_D , which is the measured deferred charge, S_{LC} is the signal level in the last pixel of the image area and N_p is the number of pixels that make up the particular row or column being analysed.

$$CTI = \frac{S_D}{S_{LC} \times N_P} \quad (7.17)$$

In these results the first 50 virtual pixel elements are summed to calculate the deferred charge, which is compared against the signal level of the last pixel of the image array and the number of pixel transfers in that column. By averaging tens of identical frames together, the shot noise experienced across pixels in the flat field image can be reduced to obtain more accurate estimates for the signal level of both the deferred charge and the signal level in the last pixel.

The EPER measurement has been used extensively and there are many examples in the literature comparing it against other methods for measuring CTE (Waczynski, et al., 2001) (Hardy, et al., 1998). The EPER measurement provides the most convenient method for calculating CTE over a large signal range relatively quickly.

7.2 CCD204 Test Device

The EPER analysis was originally carried out using the same CCD204, with the same equipment as set up for the mean-variance analysis presented in Chapter 6. However, an unforeseen effect that reduces the signal level of the last few pixels of the image area prevented an accurate analysis using the EPER method. This is described in detail in the next section. When this effect was discovered the vacuum chamber and device had been disassembled for use in other experiments. Therefore the data presented here are made using a similar equipment set-up, as used with the CCD204 measurements, but the measurements are made using a CCD273 test device. Both the CCD204 and CCD273 have been modelled during the course of this work (see Chapter 4) and because they share the same pixel geometry tests on the parallel register of one device should be comparable with the results from the other.

The tested CCD273 has previously been used as a radiation test chip in a campaign during the Euclid development cycle (Gow, et al., 2012). As such there are areas of the device which have been irradiated with protons similar to the CCD204 used in Chapter 6. This will have minimal impact on the parallel CTE measurements because these can be taken from a single column in one

of the un-irradiated control regions. However, the irradiated regions extend across the readout register, so are unavoidable in serial measurements. As such, the serial EPER measurements will not be representative of an un-irradiated CCD204 and cannot be used when comparing the measurements to the charge volume characteristics modelled in Chapter 5.

The CCD273 has a 4k x 4k imaging array that is split into four quadrants, with each having a separate output node and amplifier for fast readout. The EPER measurements presented here are made using just one of the 2k x 2k quadrants, with several hundred overscan elements, where the deferred charge measurement is taken from the first 50 virtual pixels.

The EPER measurements are made using Equation 7.17 to calculate the CTE based on the ratio of the signal level in the last pixel of the column to the amount of deferred charge in the overscan region. This is taken over the number of transfers, i.e. the length of the column. Taking the measurement from a single column or row would normally be dominated by the noise such as photon shot noise and read noise, which cause a variation in the signal level from pixel to pixel. For this reason the EPER measurements are usually made by averaging over several adjacent columns. Due to the radiation damage present in the test device, these measurements are taken from a single column in an un-irradiated control region, which is averaged from 100 identically illuminated frames to achieve a reduction in the signal level variation from pixel to pixel caused by photon shot noise and detector read noise.

7.3 EPER Measurement Technique

7.3.1 Flat Field Illumination

During the EPER measurements the CCD273 was mounted close to the end of a small vacuum chamber with a transparent window, where it was cooled using a cold-finger. The device was held at a temperature of -110°C to suppress dark current generation. An LED located outside of the vacuum chamber provided a roughly uniform illumination across the device through the vacuum chamber window. There is a gradient in the illumination level across the detector, getting brighter in the lower left corner, caused by the use of a single LED to approximate flat field illumination, (Figure 7.77).

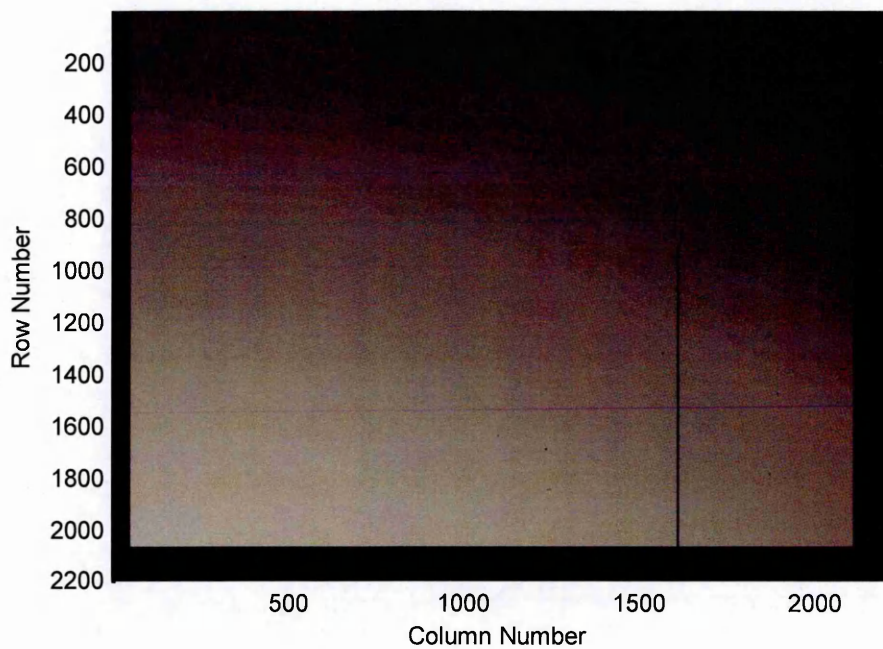


Figure 7.77: An example flat field from the CCD273 from a single 2k x 2k quadrant. A small illumination gradient is visible across the device image area. Both serial and parallel overscan regions are included in the example. Some defects are visible in the detector.

The flat field shows a slight gradient in the illumination level which is visible in Figure 7.77. Figure 7.78 shows a single column from a flat field frame, like the one shown in Figure 7.77 over a range of illumination levels. The signal level in Figure 7.78 shows that the illumination gradient across the image area becomes more severe as the illumination level increases (the brightness of the LED increases). Figure 7.78 also shows an increase in the pixel-to-pixel variance with signal size, as expected from the Poisson relationship between signal size and variance caused by the individual photons arriving at the detector over the integration time (Janesick, 2007).

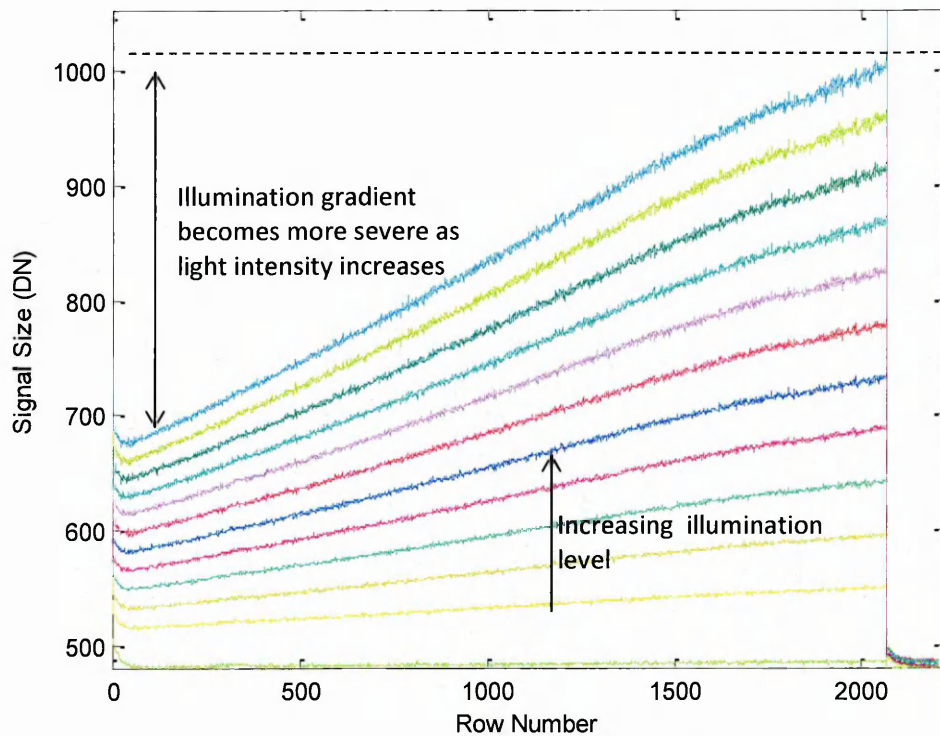


Figure 7.78: Signal level vs. row number for a range of illumination levels, showing the increasing illumination gradient in the flat field as the illumination level increases.

The LED illuminates the detector for the entire integration period, with larger signal levels produced by increasing the length of the integration time. The LED is used to illuminate the CCD273, which produces a reasonably linear signal response over the range of the integration times tested, up to the FWC of the detector which is $\sim 2 \times 10^5$ e⁻. Figure 7.79 shows the increase in the signal level in the detector, measured in the last pixel of the column over several illumination levels. The signal level of the last pixel in the column is presented because this is used in the EPER CTE calculations defined by Equation 7.17.

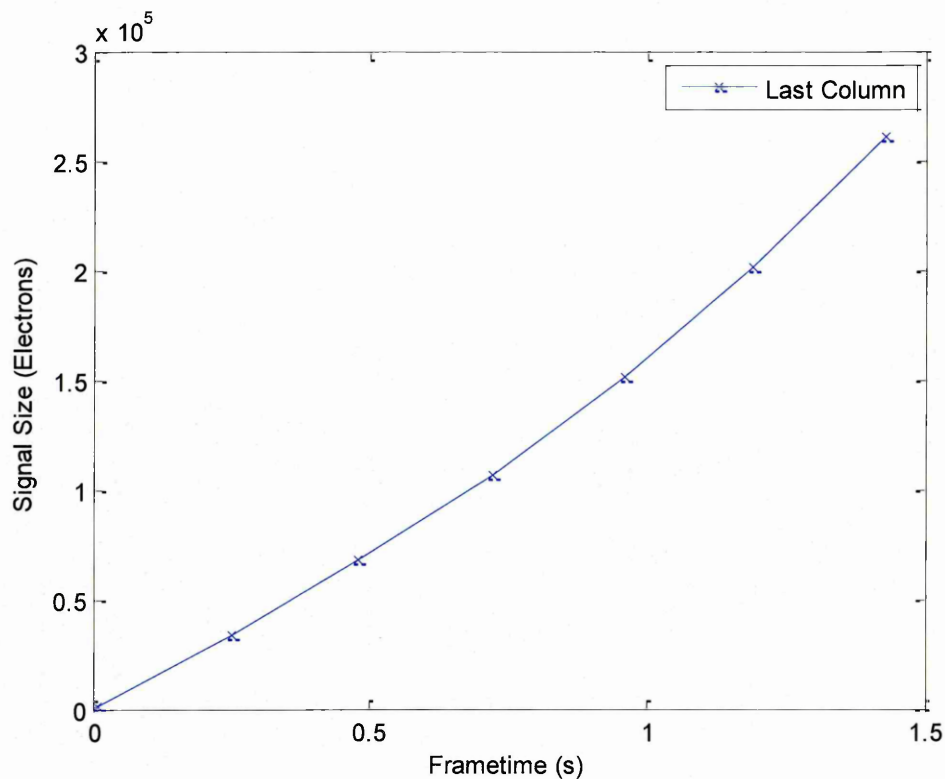


Figure 7.79: Signal level linearity produced by an LED for the last pixel in a single column from the image area of the test device. The signal level is varied by increasing the integration time, with the LED illuminated for the entire integration period.

7.3.2 Edge Roll Off

The CCD204 and CCD273 devices include a drain, an area of highly doped silicon, which runs through the middle of the active imaging area, but as these data are extracted from a single quadrant, it is located around the periphery. The drain provides a facility for charge injection, which can be used to introduce a small amount of charge into the image area and clock it through the CCD array before an image is captured. Charge can improve CTE because it will fill traps with long emission times, so that when an image is taken the charge packets that make up the image will interact with fewer traps.

Unfortunately the drain structure, which makes up the charge injection technology, causes a roll-off effect in the flat-field signal level at the edges of the device, close to the injection drain location. The drain which is an area of highly doped silicon will present a large potential sink attracting photo-electrons from the periphery of the image area. The roll-off effect can be seen in

Figure 7.80, with the last ~5 pixels of the parallel register column affected. The roll-off in signal level causes problems for the EPER measurements, because the CTE value is calculated based on the signal level of the final pixel in the array, the value of which becomes less reliable. The severity of the roll-off effect is dependent on the signal level of the flat field in question, but can represent a deviation from the flat field signal of several thousand electrons in the last pixel of the register.

The roll-off effect is the opposite of what would normally be expected from a standard CCD, i.e. a CCD without an injection drain. Standard CCDs tend to get a spike in the signal level of the last pixel in the image array because the potential well of the last pixel attracts the charge carriers which are generated in the neutral bulk material surrounding the photosensitive area (Janesick, 2007).

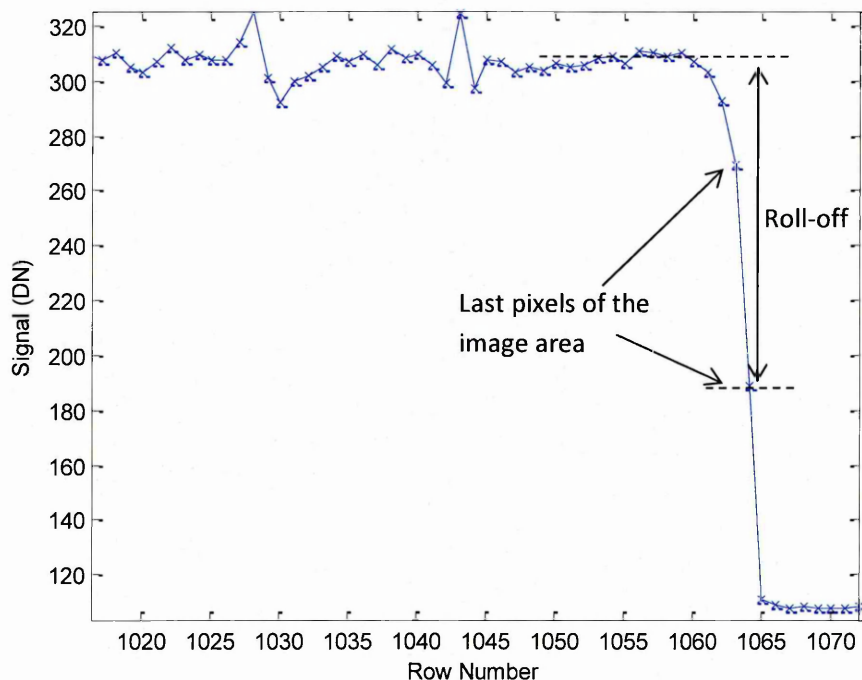


Figure 7.80: Signal level vs. pixel number from one of the columns in the parallel register, showing an example of the roll-off in signal level experienced in the last few pixels near the edge of the device. It is believed that the roll-off phenomenon is caused by the drain structures surrounding the device image area, which are used for charge injection.

The roll-off effect, Figure 7.80, can be removed from the data by modifying the readout sequence to reverse the clocking direction before a conventional readout sequence. In the modified readout sequence, charge packets are transferred in the direction opposite to the serial register causing them to pile up in the last pixel of the image array. The modified clocking sequence moves one row backwards, before the normal readout sequence is initiated. The pile up of charge packets in the last pixel of the parallel registers causes the spike in signal size seen in Figure 7.81, completely eliminating the roll-off effect which would otherwise prevent an accurate assessment of CTI from the signal level in the last pixel in the array.

The charge increases in the last pixel and is not captured by the large drain potential because the charge is located in the potential wells. The drain only affects charge accumulation during image integration, when the charge is in the process of being collected by the potential wells. Charge injection is not a common feature in CCDs and is included in the CCD273 to meet the strict CTE specifications required by the Euclid mission.

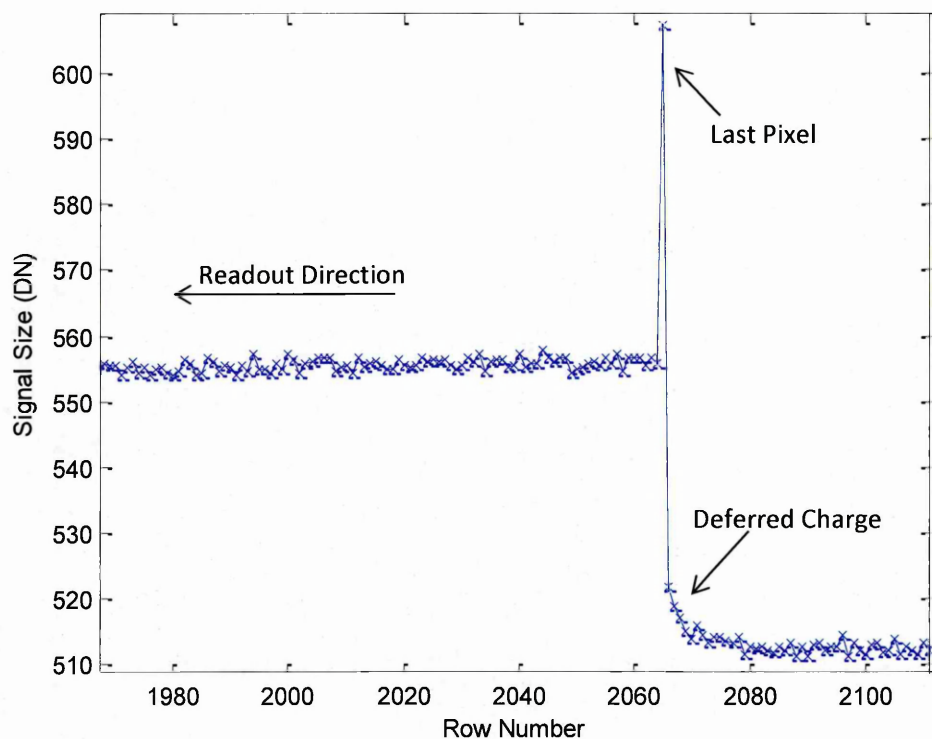


Figure 7.81: Signal level vs. row number for one column in the CCD273 showing the effect of reverse clocking one pixel away from the serial register, preventing the roll-off effect in the last few pixels of the image area.

The spike in the signal level of the last pixel of the image array, which is the result of the readout sequence, is similar to the spike which exists in standard CCDs, where the excess charge generated in the neutral bulk surrounding the detectors photosensitive area diffuses inwards and is collected in the last pixel of the array (Janesick, 2007).

7.3.3 Column Averaging

Due to the limited number of un-irradiated columns available in the test device, and the change in flat field and signal level across the device, a single column from an un-irradiated section of the CCD is used to calculate CTE. Usually EPER measurements are made by averaging across several hundred or thousand adjacent columns to reduce the noise on the signal across the imaging array. The measurements presented in this chapter are produced by averaging 100 identically illuminated frames together, reducing noise on the signal levels as seen in Figure 7.82.

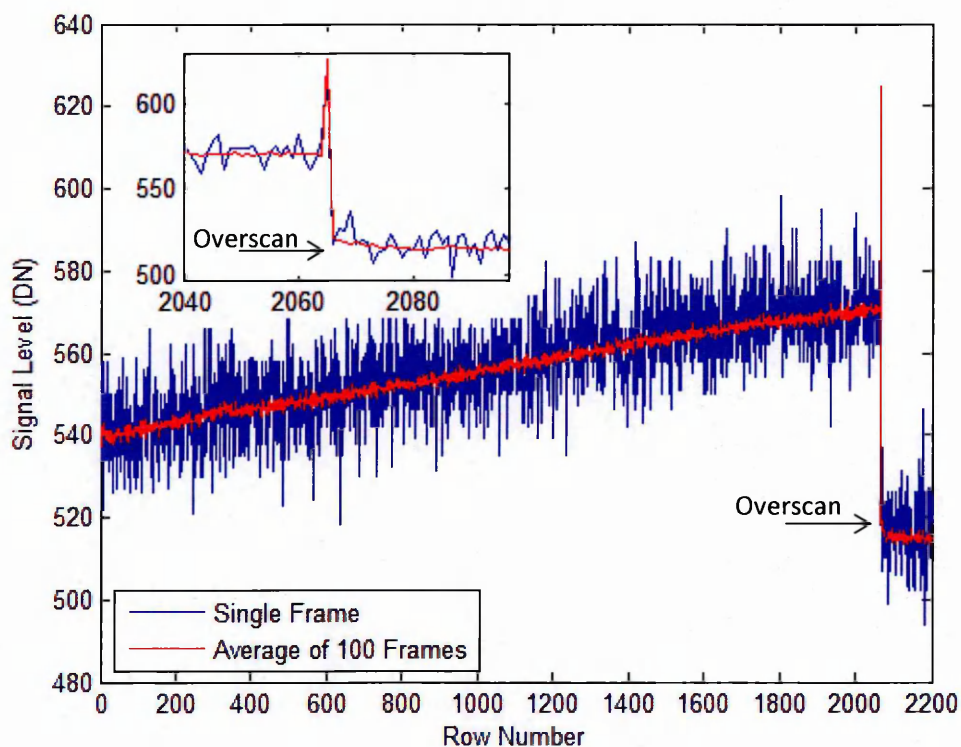


Figure 7.82: A single column taken from a flat field frame showing the variance in signal level from pixel to pixel, which is associated with the Poisson shot noise. Overlaid in red is the same column taken from a composite frame made up of an average of 100 identically illuminated frames. The averaging is done to reduce the shot noise effect and more accurately determine the signal level when considering individual pixels.

Figure 7.82 shows a variance in signal level along a single column in one frame of a flat field image. Overlaid on the same figure is the result of an average of this column over 100 identically illuminated frames. The last few pixels of the image area and first part of the overscan are enlarged and inset. Averaging many frames together in this fashion reduces the variance in signal level from pixel to pixel across the image frame, giving more accurate analysis of the signal level in a given pixel for a specific illumination level. Averaging is essential for an accurate analysis of the CTE through the EPER measurement, by reducing the uncertainty on the signal levels of the deferred charge pixels in the overscan area.

A typical column taken from the averaged image in one of the un-irradiated control regions of the CCD273 is shown in Figure 7.83. This column is illuminated over a range of signal levels to calculate parallel CTI using the EPER technique. There is only a small pixel-to-pixel variance

because each signal level is the average of 100 identical frames taken at this signal level. The gradient in signal level is not visible in Figure 7.83 because only the last few pixels of the image area and the beginning of the overscan are presented. The two highest signal levels presented in Figure 7.83 show the last pixel to be beyond FWC, evident because the signal level of the adjacent pixel, number 2064, has increased beyond the flat field level of the other pixels due to charge blooming from pixel 2065. The signal levels which exceed FWC cannot be used in CTE calculations, so these two signal levels are discarded, but each of the remaining signal levels can be used in the EPER measurements.

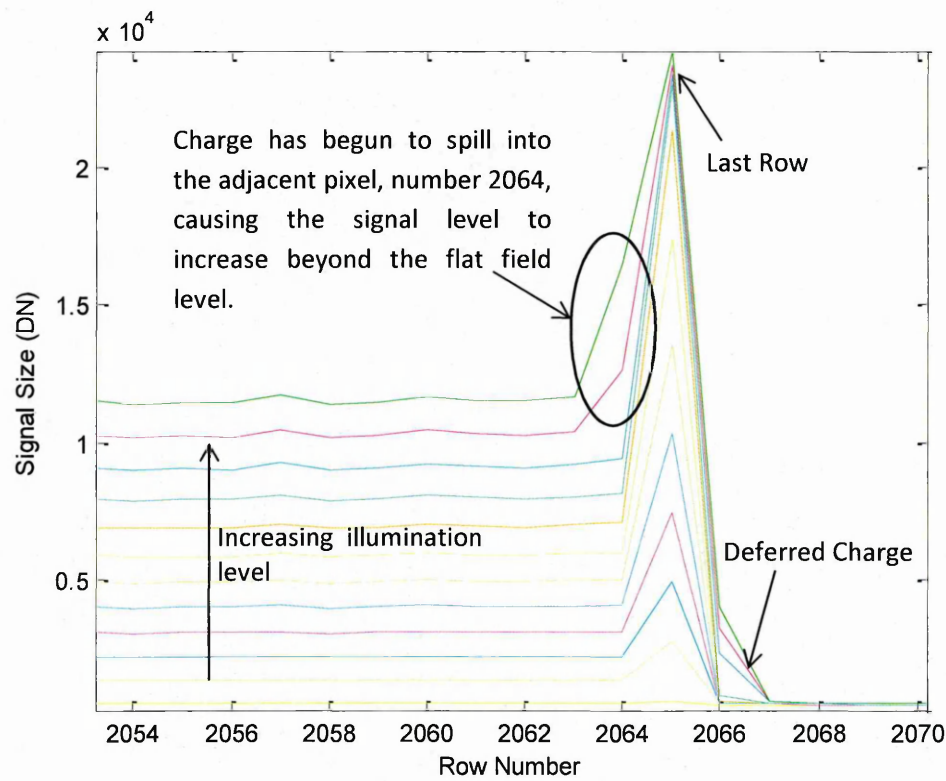


Figure 7.83: Spike in signal size of the last pixel, number 2065, caused by the backward clocking designed to prevent roll-off in this device. The two flat fields representing the brightest illumination level have a signal level in the last pixel beyond the FWC, evident as the adjacent pixel, number 2064, has a signal level higher than the flat field signal level meaning charge is blooming from the last pixel into adjacent pixels.

Figure 7.84 displays an enlarged overscan section from one of the illumination levels presented in Figure 7.83. This shows the characteristic exponential decay of the deferred charge present in the overscan region and how it is differentiated above the overscan signal level. Before the EPER calculations are performed the overscan signal level is subtracted from each of the signal levels to zero the signal level of the overscan, allowing an accurate value for the last pixel and deferred charge to be calculated.

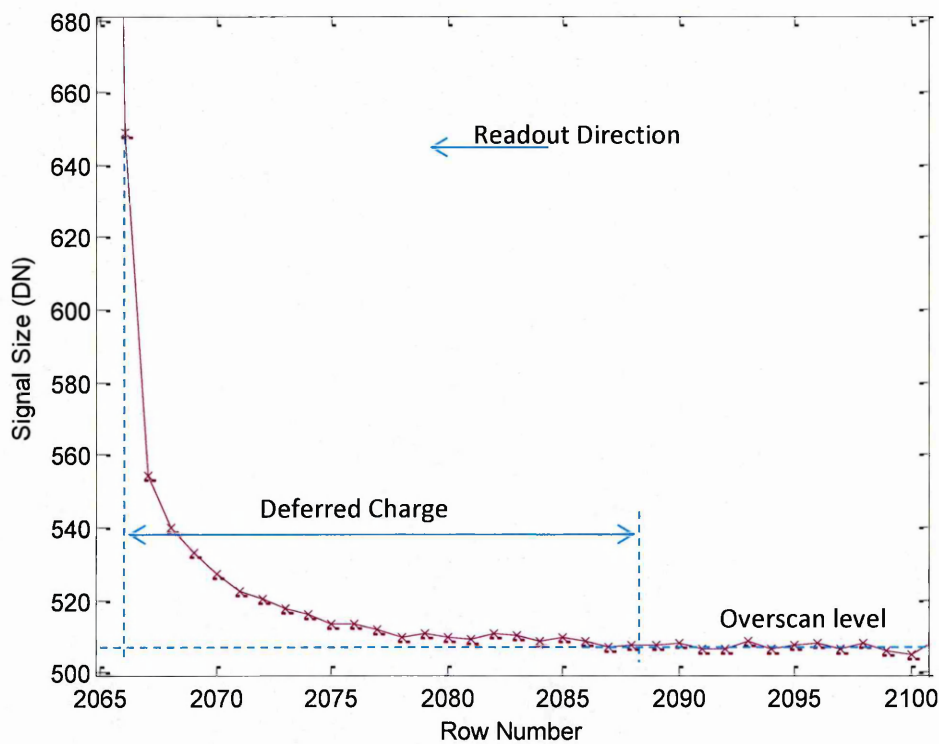


Figure 7.84: The first 35 pixels of the overscan section enlarged to show the exponential decay of the deferred charge more clearly for one of the signal levels used in the measurement.

7.4 Charge Transfer Inefficiency

Figure 7.85 shows the CTI measurements as a function of signal size calculated using Equation 7.17 with the data from Figure 7.83. CTI represents the proportion of a charge packet which cannot be successfully transferred during readout, and it shows a strong dependence on signal size. Chapter 5 discussed the possibility that the charge trapping mechanisms, and hence CTE, is dependent on the distribution of the charge packet within the buried channel. Larger

charge packets will come into contact with more traps, thus losing more charge, but compared to the larger signal size of the charge packet, the proportion of the charge loss is smaller, resulting in higher CTE.

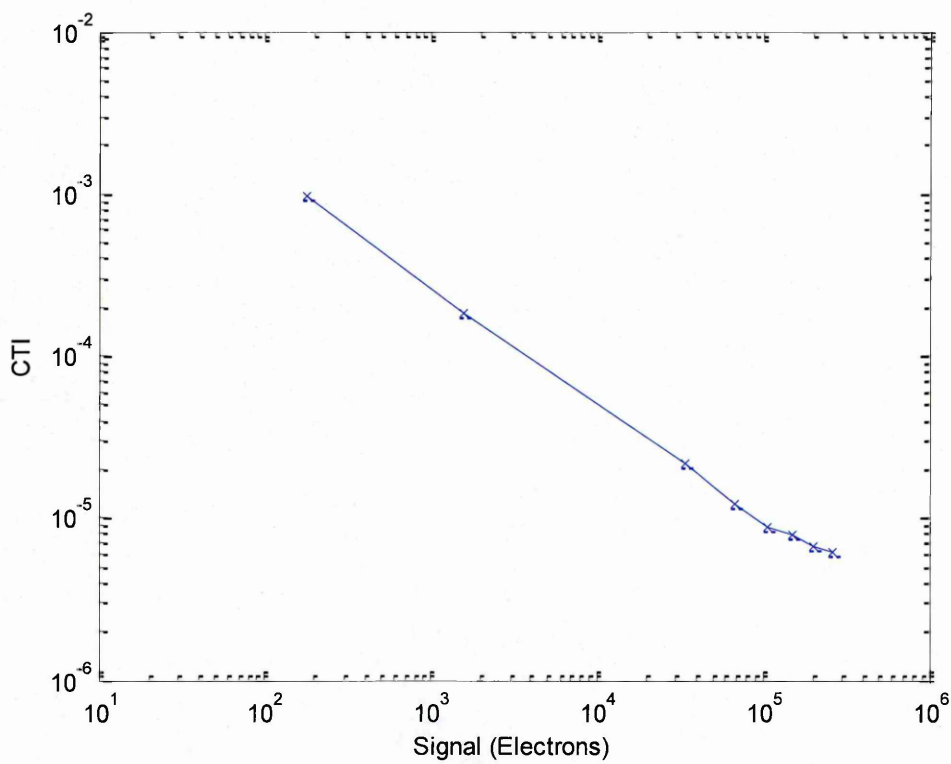


Figure 7.85: Charge transfer efficiency over a wide signal range for the CCD273 made using the EPER technique. This shows the expected CTE trend seen in other CCD studies (Hardy, et al., 1998) (Mohsen & Tompsett, 1974) and is broadly in the correct range of values with the expected distribution.

CTE is given over a log scale in Figure 7.85; the trend shows a non-linear dependence on signal level ($CTI \sim S^{-n}$: where S is signal and n produces the gradient on the log plot) as seen in previous CCD studies examining the same phenomenon (Hardy, et al., 1998) (Hopkins, et al., 1994). These measurements are taken from a single 2k x 2k quadrant of the detector, so depending on their position in the array, some charge packets may be transferred several thousand times during readout making these relatively small values of CTE significant to the accurate measurements that are required in Euclid, especially the poorer performance at low signals. These results are taken

without optimising the device for CTE, so there may be some improvements possible from optimising the transfer timings or using the charge injection structure present in this device. The high CTI at small signal is the main motivator for the charge packet models, with the aim of further understanding charge trapping and its dependence on charge distribution. Links have already been demonstrated between charge packet distributions and trapping through the use of SBCs in some scientific devices (Seabroke, et al., 2013), as discussed in Chapter 5. To compare these measurements against charge packet models the information might be better expressed as a charge loss per pixel, which is presented in Figure 7.86.

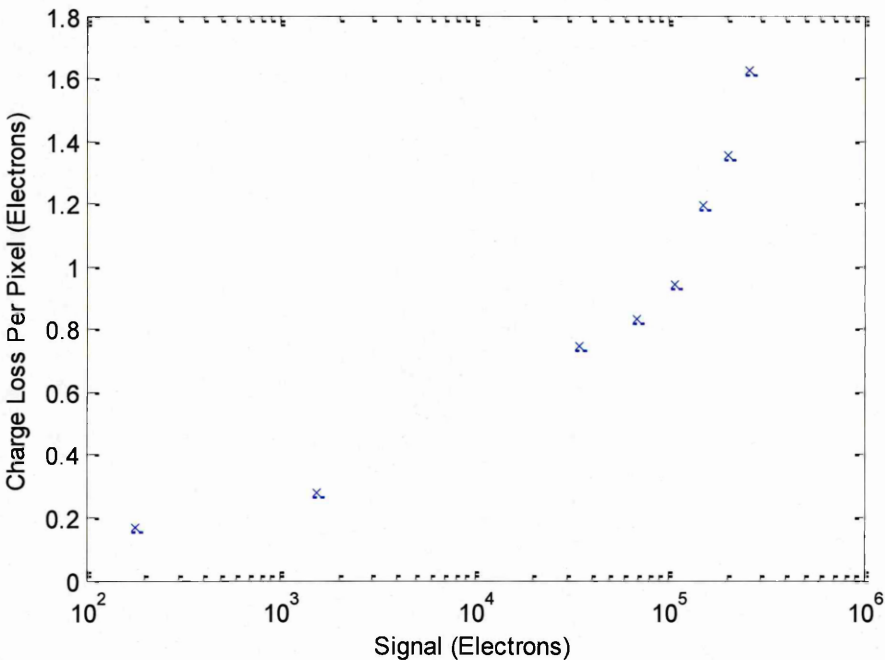


Figure 7.86: Charge loss per pixel over the signal range used to calculate CTI in Figure 7.85. Charge loss per pixel is calculated as an average from the entire column, thus values in fractions of an electron are achieved.

The charge loss per pixel shown in Figure 7.86, gives values for charge loss that are an average across entire column, the averaging results in values in fractions of an electron per pixel, which shows that traps are distributed throughout the column with fewer interacting traps than there are pixels at small signal. Charge loss per pixel is variable depending on the signal level, with larger charge loss at higher signals, resulting from the increased sizes of the charge packets, with charge

loss tending to a constant minimum at small signal levels. This distribution is reminiscent of the charge packet relationships presented in Chapter 5, which showed approximately constant charge packet volumes over lower signal levels, with charge packet volume only increasing at the higher signal levels. Figure 7.87 presents the data from Figure 7.86, with the charge packet model for the pixel from Chapter 5 overlaid.

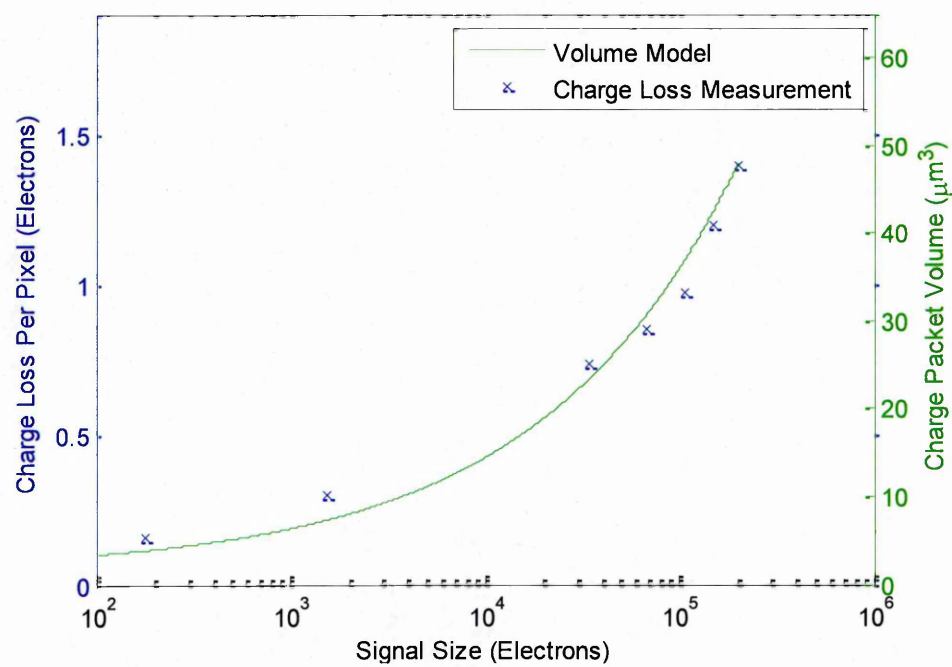


Figure 7.87: The charge loss per pixel taken from Figure 7.86, with the modelled charge packet volume from Chapter 5 overlaid and scaled using a second y-axis.

By fitting the charge packet volume, calculated from the Silvaco models, to the average charge loss per pixel, as in Figure 7.87, it is possible to calculate the density of traps in the test device. The calculated trap density can be compared to the typically expected trap density, given in Chapter 2, Table 2.1. The correlation between charge packet volume and charge loss results in a trap density of approximately $1 \times 10^{11} \text{ cm}^{-3}$, which agrees with the typical trap values from Table 2.1.

Figure 7.87 shows that the charge loss per pixel, extracted from the CTI, can be related to the charge packet volume modelled for the pixel structure in Chapter 5. The charge loss and the charge packet volume are shown to have an approximately proportional relationship, which has been suggested in previous studies (Mohsen & Tompsett, 1974). The two plots in Figure 7.87 are scaled and overlaid for comparison, where volume is measured in μm^3 , and charge loss measured in electrons. It should be noted that CTI is the result of interaction with a number of different trap types which commonly form in the bulk silicon substrate (Mohsen & Tompsett, 1974) (Waczynski, et al., 2001), but the charge volume model takes no account of charge trapping. The volume is simply defined for a specific cut-off density, which defines the boundaries of the charge packet, as described in Chapter 5. The cut-off used to define volume in Figure 7.87 is 10^{12} electrons/ cm^3 , where Figure 5.4 in Chapter 5 indicates that this density will give a high probability of capturing an electron from the charge packet if they come into contact for at least one of the common trap types.

7.5 CTE modelling

The charge packet model shows that the charge distribution is not proportional to signal size, small signal charge packets are spread out over a larger volume relative to the signal size, giving a lower average density, and thus more trap interactions occur per electron of signal. As signal level increases the charge density of the packet increases before the charge packet begins to expand. At larger signal levels the charge packets interact with more traps overall, but the proportion of traps is lower in relation to the charge packet size, causing an improvement to CTI.

Taking the charge loss model presented in (Mohsen & Tompsett, 1974), which is based on SRH theory (Shockley & Read, 1952), it is possible to run a simple analytical expression to estimate charge loss or CTE. The charge loss model shows that the number of charges held in bulk states (n_t) can be calculated using Equation 7.18.

$$n_t = N_t V_s \quad 7.18$$

Where N_t is the number of traps per unit volume and V_s is the volume of the charge packet. This is shown in Figure 7.87, where the charge packet volume has been modelled and overlaid on the charge loss data extracted from the CTE measurements. The charge loss and the charge packet volume modelled are shown to be proportional across all signal sizes ranging from tens of electrons up to FWC. Therefore by taking the charge of an electron, q , a simple relation between the charge loss (Q_{loss}) and charge packet volume is given by:

$$Q_{loss} \approx qN_tV_s \quad 7.19$$

Once the charge packet has moved away from the trap re-emission occurs and n_t reduces exponentially with the emission time constant (τ_e), which is determined through SRH theory, as presented in Chapter 2. When the charge packet is moving through a CCD register some of the charge lost may re-join the original packet, while some will only be emitted at a later time, perhaps into a trailing charge packet. Taking these factors into account the charge loss can be calculated using:

$$Q_{loss} = qN_tV_s \cdot \left(e^{(-T_{emit}/\tau_e)} - e^{(-T_{join}/\tau_e)} \right) \quad 7.20$$

This equation is taken from (Hardy, et al., 1998). Where T_{emit} is the time between one charge packet leaving and the next charge packet arriving at a point in the pixel transfer process. T_{join} is the time period during which captured charge can re-join the packet from which it was lost, where this is a fraction of the time between charge packets (T_{emit}). By substituting the charge packet volume calculated using Silvaco into V_s in Equation 7.20, charge loss can be modelled for the Euclid pixel. The charge loss model is compared against measurements in Figure 7.88.

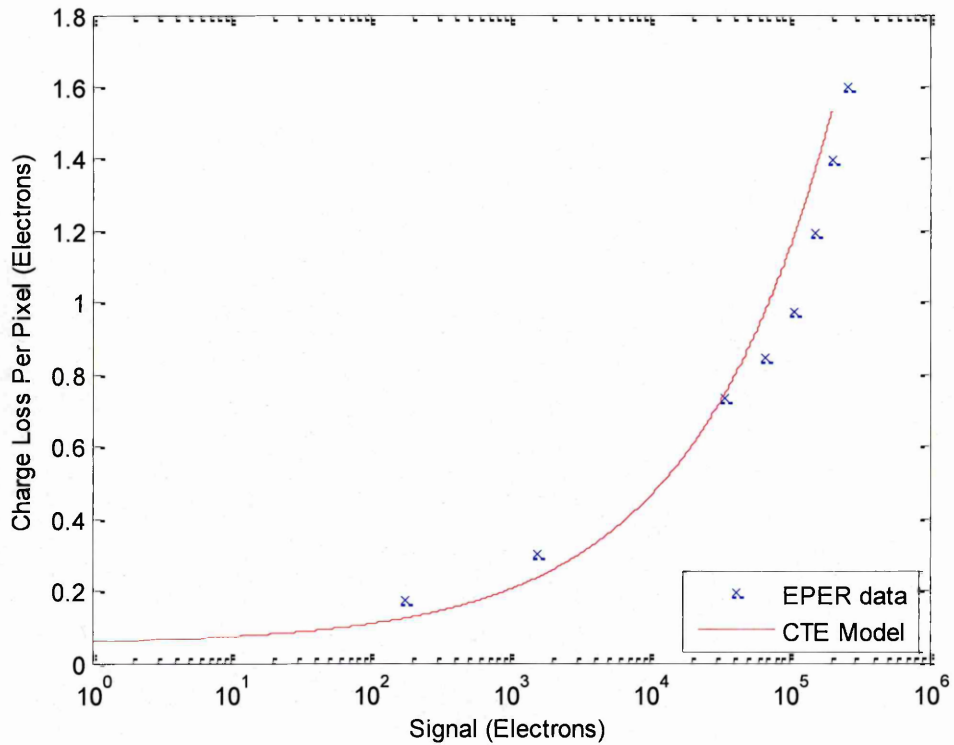


Figure 7.88: Charge loss data plotted against the charge loss predicted in the model, Equation 7.20.

7.6 Conclusions

This chapter focussed on the Extended Pixel Edge Response (EPER) measurements made using one of the two devices that were the modelling subjects of previous chapters. The measurements were initially performed on both devices, but an unforeseen side-effect caused by the injection drain present in these devices prevented accurate EPER measurements to be performed. These effects were mitigated through a modification to the readout sequence, but by the time the effect was discovered, the CCD204 test camera had been disassembled for use in other experiments. Therefore only results obtained from the CCD273 were presented.

The use of both devices in previous radiation test studies has resulted in several areas in the image arrays which have been exposed to doses of energetic protons similar to those experienced during the Euclid mission. This is not a problem for parallel CTI measurements because these can be made in un-irradiated control regions. However, the areas of irradiation extend across the

serial registers in these devices preventing measurements of serial CTE from undamaged serial registers.

The parallel CTI measured from the CCD273 using the EPER technique ties in with the results from previous CCD studies, showing a similar distribution at approximately the expected values. The results showed an expected poor performance at small signal levels which may be significant for the Euclid mission goals, but it should be noted that the results presented are obtained from a CCD which has not been optimised. The transfer timings utilised during readout are made to reflect those that have been primarily suggested for the Euclid mission, but using the 2-2-2 readout sequence that was found to perform well in Chapter 6. Improved CTE values may be obtained by optimising the transfer timings to take advantage of the trap capture and emission constants (Hall, et al., 2012), but this was beyond the scope of this study.

The CTE measurements allow charge loss per pixel to be calculated as an average across the column used to make the measurement. Charge loss is shown to increase as signal size increases in a manner similar to the change in charge packet volume shown in the device models of Chapter 5. By overlaying the data points from the charge loss measurement onto one of the trend lines developed to describe the charge-volume relationship for the pixel, an approximately proportional relationship can be observed between the two. Further analysis shows that the density of traps can be calculated by comparing the modelled charge packet volume with the charge loss per pixel, which is extracted from EPER results. These values closely match the expected trap density from previous charge trapping studies as presented in Chapter 2, Table 2.1.

Future work will be aimed at measuring the CTE in other CCD204 and CCD273 devices, preferably un-irradiated, to enable measurements of the serial CTE. The serial registers differ between the two devices, with the serial register in the CCD273 approximately x2.5 smaller than the serial register in the CCD204. This was part of a redesign aimed at improving the CTE of the serial register for Euclid. These measurements will be compared against the models in the same manner as presented in this chapter. By taking account of the differences between the two devices and

the relative difference in CTE between the two serial registers it should be possible to compare the data to the change in charge packet volume caused by the reduced channel width, as predicted from the Silvaco models.

7.7 Summary

This chapter reviewed a common measurement technique which has been utilised to measure CTE in a Euclid CCD273. The results conformed to those obtained in previous studies, showing CTE improving as the signal level increases. The results, when combined with charge models offer a method for estimating trap density, and values calculated show good agreement to common trap parameters. The change in CTE with signal size is explained in relation to the evolution of charge packet analysed in Chapter 5 and direct relationships between the charge packet volume and the charge loss are drawn.

Chapter 8: Conclusions and Future Work

This chapter summarises the conclusions which were presented as a result of the studies carried out for this thesis. Possible action for future work is also suggested for each study.

8.1 Modelling Development

Device modelling using the TCAD software packages makes it possible to model semiconductor devices by specifying device architecture, doping and biasing. Device parameters, which are well characterised in a laboratory environment, need an appropriate physical definition in the models. Analysis is usually based on the evaluation of the potential or electric field in relation to changing parameters such as electron density.

Some consideration must be given to device solutions when specifying the model mesh where memory, computational complexity and solution time need to be balanced against model accuracy. In many cases model complexity can be kept to a minimum by using dense meshing in areas where the parameter of interest will undergo a rapid variations versus position. This enables details to be captured, whilst simplifying the mesh and reducing its density in the periphery structures, which may have less-rapid spatial variations in the parameters of interest. Caution must be taken when analysing simulation results, as quantities are commonly given in atypical units and contour plots presented over logarithmic scales may be misleading.

8.2 Charge Storage Characteristics

Pixel modelling allows charge distribution to be extracted which can be used to assess the radiation performance of a device by inferring information about the probability for trap interaction through SRH theory. The Euclid CCD273 uses small pixel geometry, coupled with a narrow readout register in an attempt to achieve high CTE performance under irradiation. It is theorised that the volume occupied by the charge packet is related to charge transfer efficiency through interaction of the charge packet with traps which are evenly distributed in the buried channel. By reducing the geometry of the readout register in the CCD273 the designers hope that the charge packet will be restricted to a smaller area and will interact with proportionately fewer traps, thus improving CTE. The models are produced in Silvaco TCAD and are based on device

geometry so that the relative change between the CCD273 and the CCD204 can be calculated, with an aim to predict the relative improvement between the two devices.

The charge packet information which is output from the device models is in the form of electron density vs. position. This allows the charge distribution to be processed using the SRH equations for analysis of the trapping probability vs. position for specific traps. Alternatively the charge packet volume can be estimated directly by choosing a charge density value to define the edge of the charge packet, based on the capture probability of common traps and transfer timings during operation, and calculating its extent in each dimension.

The Charge Distortion Model (CDM) describes the two model methodologies used in the Gaia CTE campaign to try and predict the charge packet distribution, although neither the volume driven model nor the density driven model described by this function could explain some of the observations made in the Gaia test campaign. These earlier models take no account of device architecture but are calibrated against empirical observations. An optimised signal-volume model is presented which is derived from the charge distributions modelled in the Silvaco simulations. Silvaco Models are directly related to the physical structures of the CCD and so present a much clearer view of the evolution of the charge packet. In some cases, at small signal, the charge packet may not reach a density which can be measured using the method described – in these cases the plots can be incomplete and rely on the extension of the trend line beyond the values calculated from the models.

A mathematical function similar to that used in the CDM for Gaia, but with some modifying constants, is fitted to the signal-volume data to describe the evolution of the charge packet as signal size increases. This fit varies between structures with differing geometries, showing that larger devices are generally more dispersed. The charge packet volumes described by the CDM tend to match Silvaco output at large signal, for specific β parameters but there is a large divergence at small signal.

The Silvaco models have shown that the charge packets are confined to a finite volume determined by the lateral extent of the potential field which is controlled by the gate geometry, and the potential well which forms across the depletion region. Charge packets with a small signal level tend to occupy a disproportionately large volume, and this tends to vary depending on the structure geometry, with larger structures showing larger volumes, at lower average densities, for the same signal size.

The charge packet is more dispersed in larger structures because the potential well reaches its maximum channel potential and charge in the centre is less likely to be influenced by the fringing fields at the electrode edges. The charge packet tends to be a distribution of charge with a higher density in the centre and gradually reducing over a finite distance towards the edges of an electrode, resulting in the typical 'charge cloud'. As signal size increases so do both the density and volume of the charge packet until full well capacity is reached, when charge will no longer be confined to the potential well.

The Gaia mission attempted to mitigate the CTE effects by introducing a Supplementary Buried Channel into the parallel registers. The SBC was introduced because the Gaia pixels are much larger than those used in Euclid, $\sim 30\text{ }\mu\text{m}$ across. SBCs have been shown to improve CTE due to the restriction of the charge packet to a much narrower buried channel, proving the link between CTE and charge packet distribution. In the last section of this chapter, the effects of a hypothetical SBC in the Euclid pixel were explored as part of the Euclid device development, although the inclusion of an SBC was unlikely due to the already small size of the Euclid pixel, resulting in a minimal performance gain, and the late stage in the design process. The models showed that the SBC tends to improve CTI at small signal levels, until the SBC becomes saturated and charge spills into the wider buried channel. While an SBC does reduce the volume at small signal, the volume at large signal is relatively unaffected. The inclusion of an SBC, whilst improving small signal performance, complicates the relationship between signal size and charge packet distribution, potentially degrading the ability to correct images.

8.3 Factors Affecting Full Well (Model Verification)

As part of an effort to improve and verify the model results, an in-depth study into the FWC of the CCD204 test device was made. FWC is a device parameter which is highly sensitive to a number of factors. Some of these are variables which are fixed at the time of manufacture, such as pixel architecture (i.e. gate dimensions) and doping, but also operating parameters, such as the operating voltage or the readout sequence which can be optimised during device characterisation.

A number of the factors which may affect FWC have been explored in this chapter in an effort to verify device models where FWC has been simulated. The first set of results, measuring FWC over range of operating voltages, showed the simulated FWC to consistently overestimate the parameter when compared against the measurement values. These overestimates were assumed to be caused by the suspected over-etch observed in the electrode structures seen during the FIBSEM analysis. These might equally have been caused by some unforeseen effect of the dynamic potential field during readout, further testing was necessary.

The tests which explored the operating voltage highlighted the effect which using different readout sequences can have on the FWC measured in the test device. Two sequencers were tested, the first resembling the planned readout sequence for the Euclid mission. This was a 3-2-3 readout sequence, possible because the image area is a four phase design, where the numbers represent the number of gates which are biased during each stage of the transfer process. The second sequencer tested was a 2-2-2 sequence which produced much improved measurements and indicated a channel parameter and an optimum operating voltage of approximately 9-10V. The fact that the FWC varies depending on how on how the device is operated potentially makes model verification difficult.

Investigations into the device geometry through the FIBSEM analysis is presented to give an indication of the gate dimensions in a CCD273, which should share the same gate dimensions with the CCD204. Gate dimensions have a direct impact on charge packet dimensions and hence FWC, so any deviation from design will affect the modelling performance. The images are taken from a

reject CCD273 wafer, the reject was used because FIBSEM imaging is a destructive process. The results provided an indication that the manufacturing process is not providing the designed gate dimensions with an over-etch in at least one poly-silicon layer. However, adjacent gates tend to take up the extra space created by the over-etch and compensate for the undersized poly- layers preventing any indication of this manufacturing variation during normal operation of the devices. Other device dimensions such as the inter-poly oxide and the gate deposition thickness seem to closely follow the design specifications with little variation. The deviation from the design gate dimensions indicated by the FIBSEM images is worked into the device models to improve the relationship between model output and test measurements.

In an attempt to tie measurements and models together further tests were conducted by modifying the software readout sequencer to measure FWC using only a single image collecting phase. This test was repeated for each of the of the four image phases to note any changes between the FWC in each image phase. If the test device followed the design criteria two distinct FWCs should have been measurable across the four phases. However, three separate FWCs were measured indicating that the device electrodes have been deposited to three separate widths, instead of the two different widths which were expected.

By using the FIBSEM measurements to modify the device models the FWC was re-simulated for individual gates in models which reflected both the design dimensions and the FIBSEM measurements. The results from these models were presented and compared against the measurements from the test device which form a much closer agreement indicating that an over-etch is very likely to exist in this device. Assuming that the models are correct, they now offer a method of calculating the gate dimensions from the FWC measurements. Using this method on values taken from the test device, gate dimensions can be predicted for each of the four phases. The total pixel pitch using each of the predicted gate sizes is very close to the design pitch of 12 μm when inter electrode gaps are also taken into account, giving high confidence in the results.

It should be noted that owing to this work e2v have revised their manufacturing process to correct for the miss-sized gate dimensions. A repeat of the FIBSEM analysis on a device from the new manufacturing process is planned.

8.5 Charge Transfer Efficiency (EPER)

Extended Pixel Edge Response (EPER) measurements were made using a CCD273 which has been modelled in previous chapters. The measurements were initially also performed on the CCD204, the subject of the FWC tests in Chapter 6, but an unforeseen side-effect caused by the injection drain present in these devices prevented accurate EPER measurements to be performed. These effects were mitigated through a modification to the readout sequence, but by the time it was discovered, the CCD204 test camera had been disassembled for use in other experiments. Therefore only results obtained from the CCD273 were presented.

Unfortunately the use of both test devices in radiation studies has resulted in several areas in the image arrays which have been exposed to high doses of protons to intentionally damage the detectors for Euclid characterisation (Gow, et al., 2012). This is not a problem for parallel CTI measurements because these can be taken from un-irradiated control regions present in the devices. However, the areas of irradiation extend across the serial registers in these devices preventing measurements of serial CTE from undamaged serial registers.

The parallel CTI measured from the CCD273 using the EPER technique ties in with the results from previous CCD studies (Hardy, et al., 1998) (Waczynski, et al., 2001), showing a similar distribution at approximately the expected values. The results showed poor performance at small signal levels, but it should be noted that the results presented are from non-optimised device operation. The transfer timings utilised during readout are made to reflect those which have been primarily suggested for the Euclid mission, but using the 222 readout sequence which was found to perform better than the Euclid's suggested 323 sequence in Chapter 6.

The CTE measurements allow charge loss per pixel to be calculated as an average across the column used to make the measurement. Charge loss is shown to increase as signal size increases

in a manner similar to the change in charge packet volume shown in the device models of Chapter 5. By overlaying the data points from the charge loss measurement onto one of the trend lines developed to describe the charge-volume relationship for the pixel, an approximately proportional relationship can be observed between the two. As signal, and hence the charge packet volume increase, so too does the level of charge loss caused by trap interaction, with the two trends are shown to match very closely. By comparing charge loss to the simulated charge packet volume it is possible to estimate the density of traps present in the detector. Comparing the trap density to the expected trap density, from Chapter 2, the values are very similar. Charge packet volume is proportional to CTE in many analytical CTE equations. The latter sections of this chapter explored a common CTE model, which is used to calculate charge loss, for comparison against measured values.

8.6 Future Work

There are a number of possible directions for future work. Initially studies will be used to further develop confidence in the models, through further testing of common device parameters and FWC. Testing of FWC values in the serial registers against those predicted from Silvaco models will also require further experimental testing to produce PTCs for serial registers. Further FIBSEM investigations are also planned to check the effectiveness of the new manufacturing process which was developed to correct the gate dimension errors.

More work will be aimed at measuring the CTE in other CCD204 and CCD273 devices, preferably un-irradiated, to enable measurements of the serial CTE. The serial registers differ between the two devices, with the serial register in the CCD273 approximately x2.5 smaller than the serial register in the CCD204. This was part of a redesign aimed at improving the CTE of the serial register for Euclid, with charge confined to a smaller channel, fewer trap interactions will occur. By taking account of the differences between the two devices and the relative difference in CTE between the two serial registers it should be possible to compare the data to the change in charge packet volume caused by the reduced channel width, as predicted from the Silvaco

models. Finally, work will commence to integrate the findings of the device models into existing CTE models, in an effort to further understanding trapping effects on device operation.

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